Series 16

HARDWARE DOCUMENTATION

MODEL H316/06
Memory Expansion Option

INSTRUCTION MANUAL

This manual contains a detailed description of the option for expanding the memory sizes of the H316 General Purpose Computer from 16K to 32K. Also included are logic block diagrams and special module descriptions.

DOC. NO. 70130072276H ■ ORDER NO. M-474 ■ JUNE 1973

Honeywell

REVISION HISTORY

New Revision Level of Manual	Change No.	Effective Date	Number and New Revision Level of Affected Drawings	Pages Affected by Revision
B	8458	July 1970	70025827B 70025828B 70025834B	21 17 19
C	8538	July 1970	70025825B	15
D	8675	Nov. 1970		A-1, CC-510A, 1 thru 5, CM-490, 1 thru 5
E	9490	June 1971	-- C70025825C C70025827C	iii, iv, 1, 2, 7 15 21
F	20687	Dec. 1972	-- C70025825D C70025828D C70025834E C70025827E C70025831B C70025826D C70025833B C70025830B C70025832B	iii, iv, 1, 2, 3, 4, 7, 8, 9, 10, 12 thru 15 17 19 21 23 25 27 29 31 33
G	20362	Mar. 1973	70024622C	CC-819A
H	30162	June 1973	C70025825E	17

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H316-0601/0602
MEMORY EXPANSION

INTRODUCTION

This document contains a detailed description of the option for expanding the memory sizes of the H316 from 16K through 32K in 4K increments. Model H316-0601 provides the necessary logic in the central processing unit (CPU) for addressing and data transfer from the expanded memory. Model H316-0602 provides the logic to control memory above 16K.

Reference Data

H316 Central Processor Description, Doc. No. 70130072176, H316 Central Processor Instructions and Logic Diagrams, Doc. No. 70130072174, and H316 Circuit Modules and Parts Manual, Doc. No. 70130072166.

Physical Characteristics

The Memory Expansion logic consists of a printed circuit board located in the CPU main frame which is H316-0601 and a 1 x 3, in addition to the required memory, located in the option drawer. The 1 x 3 is H316-0602.

Functional Description

The H316-0601 option increases the size of the P-register and Y-register to 15 bits and introduces an extend mode (for extended addressing) for memory expansion above 16K. The added P-register bit (P02) provides the fifteenth bit necessary to provide access to a 32K address field. The extend mode changes the interpretation of the index bit of the indirect address word to provide a fifteenth address bit. It also provides the logic to drive signals to the option drawer and receive signals from the option drawer when H316-0602 is installed. The H316-0602 contains a data register and memory timing and control logic.

Installation

The μ-PAC types and their locations in the option drawer are shown on LBD 0.005. The connection points for the memory cables and central processor connectors are shown on LBD 0.004 and 0.008, respectively.

H316-0601

Memory expansion above 16K is achieved by increasing the 14-bit address held in the P- and Y-registers to 15 bits so that 2^{15} or 32,768 possible locations can be addressed. When the sector addressed is other than sector zero, bit 2 of the Y-register is conditioned by bit 2 of the P-register to access locations higher than 16K. See Table 1 for a list of signal mnemonics and definitions.

Table 1.
Function Index

Mnemonic	Definition
BANKA-	Bank signals to memory
BANKB-	Bank signals to memory
BANKC-	Bank signals to memory
BANKD-	Bank signals to memory
DREDY-	Timing signal gating the data register into the M-register
DREST+A	Data register reset
LOADD+A	Load address into memory
LDTR+A	Load M-register into data register
MARCC-A	Memory address register reset
MARCC-B	Memory address register reset
MADnn-	Memory address sent to memory
MAInn+	Memory address mnemonic in the 1 x 3 from the CPU
MBUSY	Memory busy
MCTnn+	Delay line taps
MDInn+	M-register power up bits - 1 x 3 mnemonic
MDOnn+A	Data register 1 x 3 mnemonic sent to CPU
MDOnn+	Data register 1 x 3 mnemonic sent to memory
MEMCI+	Memory cycle initiate 1 x 3 mnemonic
MEMnn+	M-register power up CPU mnemonic
MMCYI+	Memory cycle initiate CPU mnemonic
MnnFF-	M-register bits
MMDnn+	Data register bits CPU mnemonics
MMEND-	End of memory cycle
MREAD+	Read/Write command
MSTRB-	Memory strobe
MXTMG+	X Read/Write timing
MYTMG+	Y Read/Write timing
MnnAD+	Memory address CPU mnemonics sent to 1 x 3

Table 2 gives the user of this manual a cross-reference list of the different mnemonics used for the same signal in the memory expansion 1 x 3 BLOC and the H316 main frame drawer. It also provides a cross-reference list for different mnemonics of signals used in the memory expansion 1 x 3 BLOC and the individual memory modules.

Table 2.
Cross-Reference List of Signal Mnemonics

Memory Expansion 1 x 3 Mnemonic	H316 Main Frame Mnemonic
MAInn+	MnnAD+
MDInn+	MEMnn+
MDOnn+A	MMDnn+
MEMCI+	MMCYI+

Memory Expansion 1 x 3 Mnemonic	Memory Module Mnemonic
BANKn-	BANK-n
MADnn-	MADXX+
MARRC-X	MADCL-X
MBUSY+	MBSYX+
MDOnn+	MnnFF+
MMDnn-	MMnnF-
MSTRB-	STROB-
MXTMG+	XTIMG+
MYTMG+	YTIMG+

Access to locations in the alternate 16K from that in which the current instruction is stored is a function of the extend mode. The control logic for extended addressing is shown in LBD 0.136 at the back of this manual. This option also contains memory timing and a data register for the additional memory and the logic to power and DJ the M-register.

The extend mode changes the interpretation of the index bit of the indirect address word, which becomes part of a 15-bit indirect address. Only one level of indexing is possible in the extend mode. It is specified by bit 2 of the instruction word and is always the final operation in generating the effective operand address.

The entry to and exit from the extend mode is under program control; however, entry into the extend mode is also gained with the occurrence of any program interrupt. A monitor flip-flop (PMIND, LBD 0.136) retains the mode in which the computer is operating when a program interrupt occurs. PMIND is set if the CPU is in the extend mode when a priority interrupt occurs. It is reset if the CPU is not in the extend mode when a priority interrupt occurs or if the MSTR CLEAR pushbutton is depressed.

Figures 1, 2, and 3 are flow charts which illustrate the modifications made to the fetch (F) and indirect (I) cycles of a machine with memory expansion. Indexing is forced to occur after indirect addressing as a function of signal M02DJ+. This signal replaces M02FF+ at the input of gate EXSTL- (LBD 128) of the central processor unit, to inhibit the

generation of signal EXSTL. Signal EXSTL is used to enable the contents of the X-register to summand G in the CPU sum network (see LBDs 101 through 116*) for indexing.

The state of M02DJ+ is controlled by the inputs to five gates (LBD 0.136). For the generation of M02DJ+, at least one input to each of the five gates must be at ground in order for M02DJ+ to be +6V. The inputs to gate M02DJ+D tell us that if the CPU is not in the extend mode and M02 of the instruction or indirect address word is a ZERO (indexing not called for), M02DJ+ will be forced to ground, thus inhibiting indexing. If, on the other hand, M02 of the instruction word is a ONE, M02DJ+ will be at +6V, enabling indexing. Note that, when not in the extend mode, indexing is a function of the state of M02 as is the case in a CPU without the extend mode capability.

The inputs to M02DJ+C inhibit indexing when indirect addressing is called for in the extend mode. This condition exists for successive I-cycles and is dependent, while in the extend mode, on the state of the flag bit (M01).

When indirect addressing is not called for during an extend mode F-cycle, the state of M02DJ+, and as a result, the requirement for indexing, is a function of the inputs to gate M02DJ+B. If the FCYM2 flip-flop is set or the tag bit (M02) is a ONE, indexing is permitted.

The inputs to gate M02DJ+A inhibit indexing, while in the extend mode, if the CPU is an I-cycle and flip-flop FCYM2 remains reset (indexing was not called for in the original instruction word). Gate M02DJ+ prevents indexing on indirect LDX (LSX0p), whose address is greater than 16K, while in the extended mode (EXTMD set).

Signal BSICY- (LBD 0.136, D7) is used (LBD 102, B9) to inhibit the state of M02 from controlling the adder during an I-cycle when not in the extend mode. Similary, signal EXTMD- (LBD 0.006, B10) inhibits the state of M02 from entering the adder during the A-cycle of a JST instruction while in the extend mode. Gates H02DJ+ and H02DJ+A (LBD 0.136) provide additional inputs from P02 to summand H of the CPU sum network for these cases.

Referring to LBD 0.006, note that diode cluster BSH02 is added for memory expansion. This gate forces M02 to be replaced by P02 when in the extend mode. When in the extend mode, EXTMD- is at ground, inhibiting M02 at gate BSH02; however, gate H02DJ+A (LBD 0.136) is not inhibited and performs the function of grounding H02DJ+ as do gates EXTM2- (LBD 263) when the memory lockout option is used.

A program can operate in either the upper or lower 16K of memory with EXTMD reset, but it cannot address across the 16K division. P02BS controls the state of Y02FF with EXTMD flip-flop reset (see LBD 102). P02BS is updated every F cycle regardless of the state of the EXTMD. Therefore, it reflects the condition of Y02FF during the last fetch. Only with EXTMD set can Y02FF be different from P02BS (see LBD 102) and the 16K division crossed.

When an interrupt occurs and the interrupt routine is initiated (forced JST), CLRF5 sets EXTMD and strobes the state of the control flip-flop SEXTF- (LBD 136, G1) feeding EXTMD into PMIND (previous mode indicator PMIND+ (LBD 136, N1).

*Doc. No. 70130072174

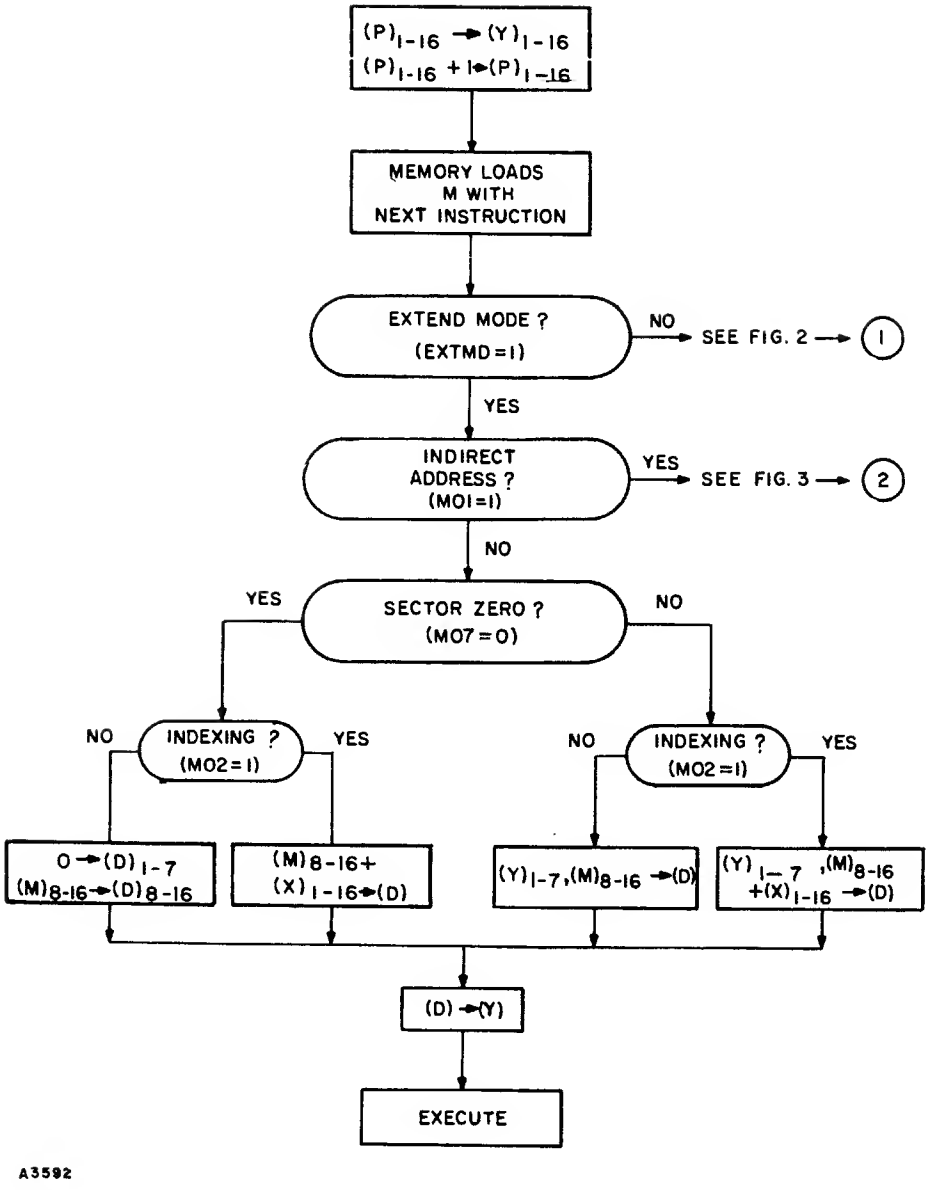


Figure 1. Operation of a System with a 32K Memory, Flow Diagram

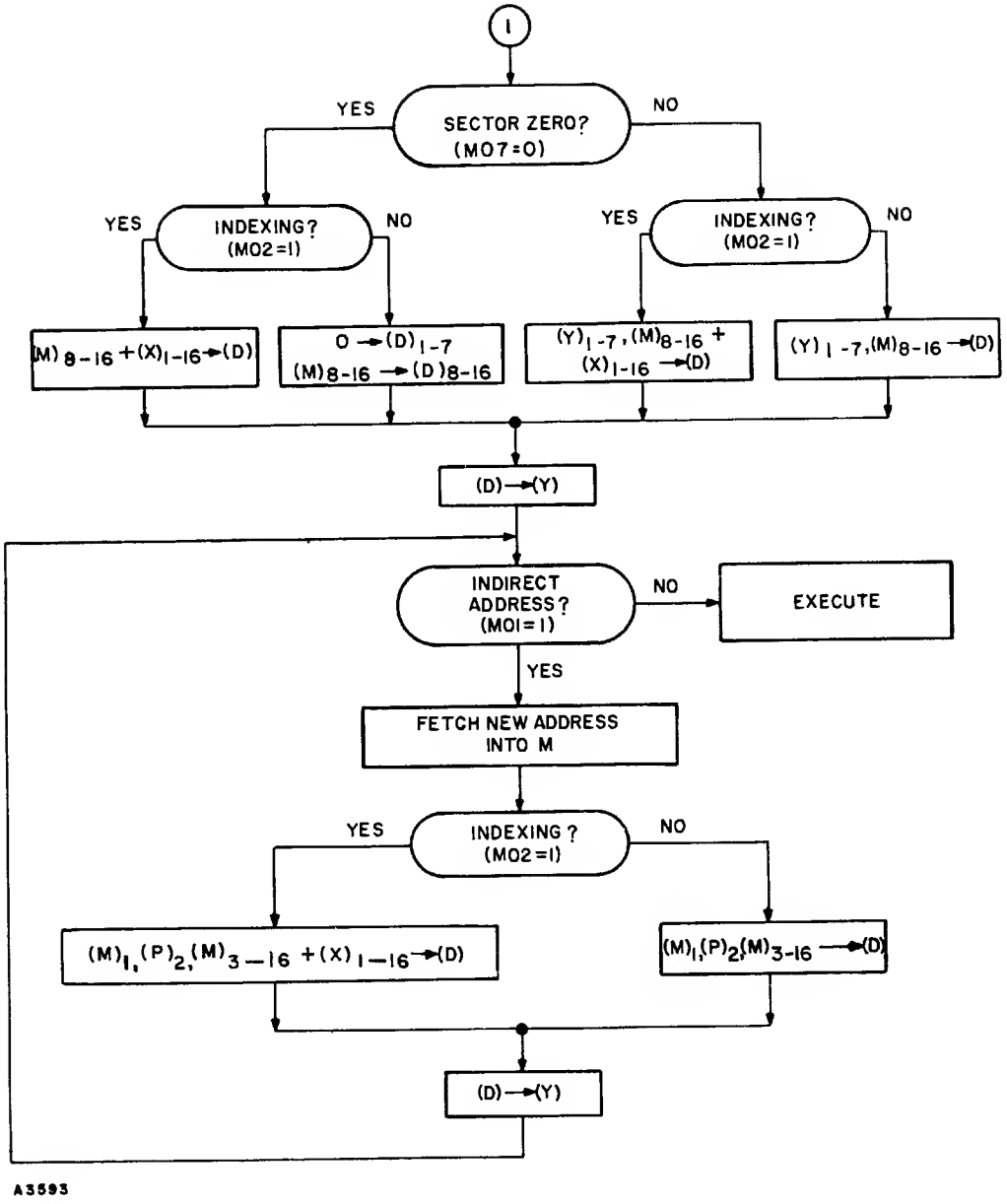


Figure 2. F- and I-Cycles Without Extend Mode Flow Diagram

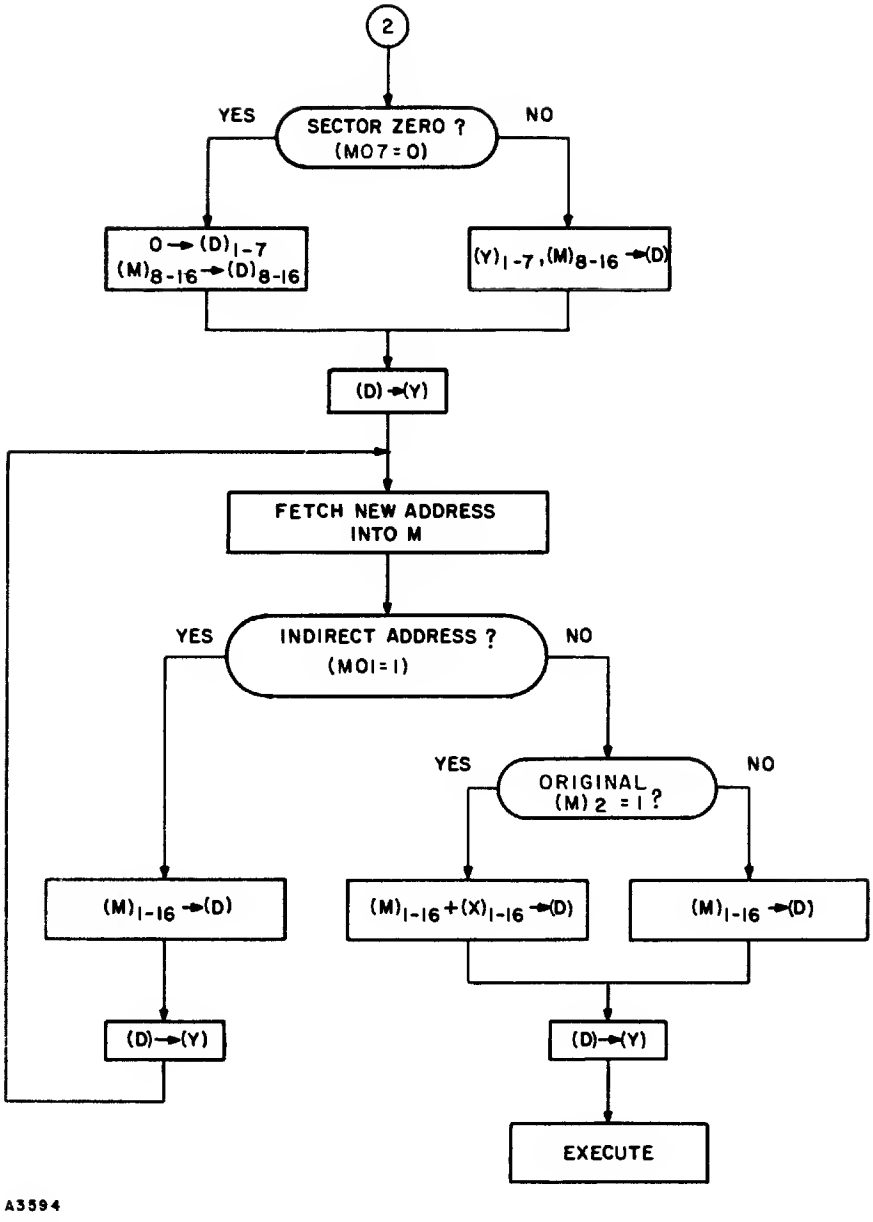


Figure 3. Indirect Addressing in Extend Mode
Flow Diagram

The state of this PMIND as well as the state of some other function is stored in the CPU A-Register if the interrupt routine contains an INK (input keys) instruction. (See H316 Central Processor Instructions and Logic Diagrams, Doc. No. 70130072174.)

At the end of the interrupt routine, an OTK (output keys) instruction can be executed to restore the functions to their original states. For example, signal STEXT is generated as a result of OTK to set the EXTMD flip-flop at the next TL1.

H316-0602

The memory timing and control 1 x 3 provides the necessary timing signal to operate an additional 17K of memory. The 1 x 3, in addition to the timing signals, also contains address gating and a data register.

All timing and control signals are generated on LBD 0.000. A memory cycle is generated by MEMC+ and address bit 2 (MAI02+) being high. This sets the MEMFF flip-flop sending a negative going pulse down the delay line. Various combinations of delay line taps develop all the timing signals (refer to LBD 0.000). MEMFF is reset by RESET- which allows about a 400 ns pulse down the delay. This generates one-half of the cycle, the other half of the cycle is started by RSTRT- which sets the MEMFF, which is then reset by RESET-.

During a read-restore operation, MREAD+ will be high allowing a strobe pulse MSTRB- to be generated. Data out of memory MMDnn- will set data register bits MDOnn+ which are sent to the mainframe and strobed into the M-register by DREDY-. MDOnn+ is also returned to memory, restoring the data in memory.

During a clear-write operation, MREAD+ is low inhibiting the generation of MSTRB- and generates LDATR+A which strobes M-register data MDInn+ into the data register MDOnn+. MDOnn+ is then sent to memory to write data into memory.

For each cycle MDOnn+ is reset at the beginning of the cycle by DREST+A and the address and bank signal is gated to the memory by LOADD+A.

INSTRUCTION COMPLEMENT

Enable Extended Addressing (EXA)

Type: G, 1 cycle

Op Code: 000013

Function: This instruction places the computer in the extend mode. (See Figure 4, Memory Expansion Detailed Flow Chart, and Table 3, Memory Expansion Analysis.)

Disable Extend Mode (DXA)

Type: G, 1 cycle

Op Code: 000011

Function: This instruction restores the machine to normal mode. The mode change is not effective until after a JMP instruction has been executed. Any number of non-JMP

instructions may be included between the DXA and the first JMP instruction. The purpose of this feature is to allow the computer to exit from an interrupt subroutine. Master Clear also disables the extend mode. (See detailed flowchart and analysis, Figure 4 and Table 3, respectively.)

The following instructions are modified.

Jump and Store Program Counter (JST)

The extend mode alters the JST instruction to allow it to store a 15-bit program counter. Bit 1 of the memory location specified by the effective operand address is left unchanged.

Input Keys (INK)

Installation of Memory Expansion modifies INK to include the copying of the PMI flip-flop contents into bit 3 of the A-register.

Output Keys (OTK)

Installation of Memory Expansion modifies OTK to include the enabling/disabling of the extend mode if bit 3 of the A-register is set/reset. (Effectivity of the disabling action is identical to that described for the DXA instruction.)

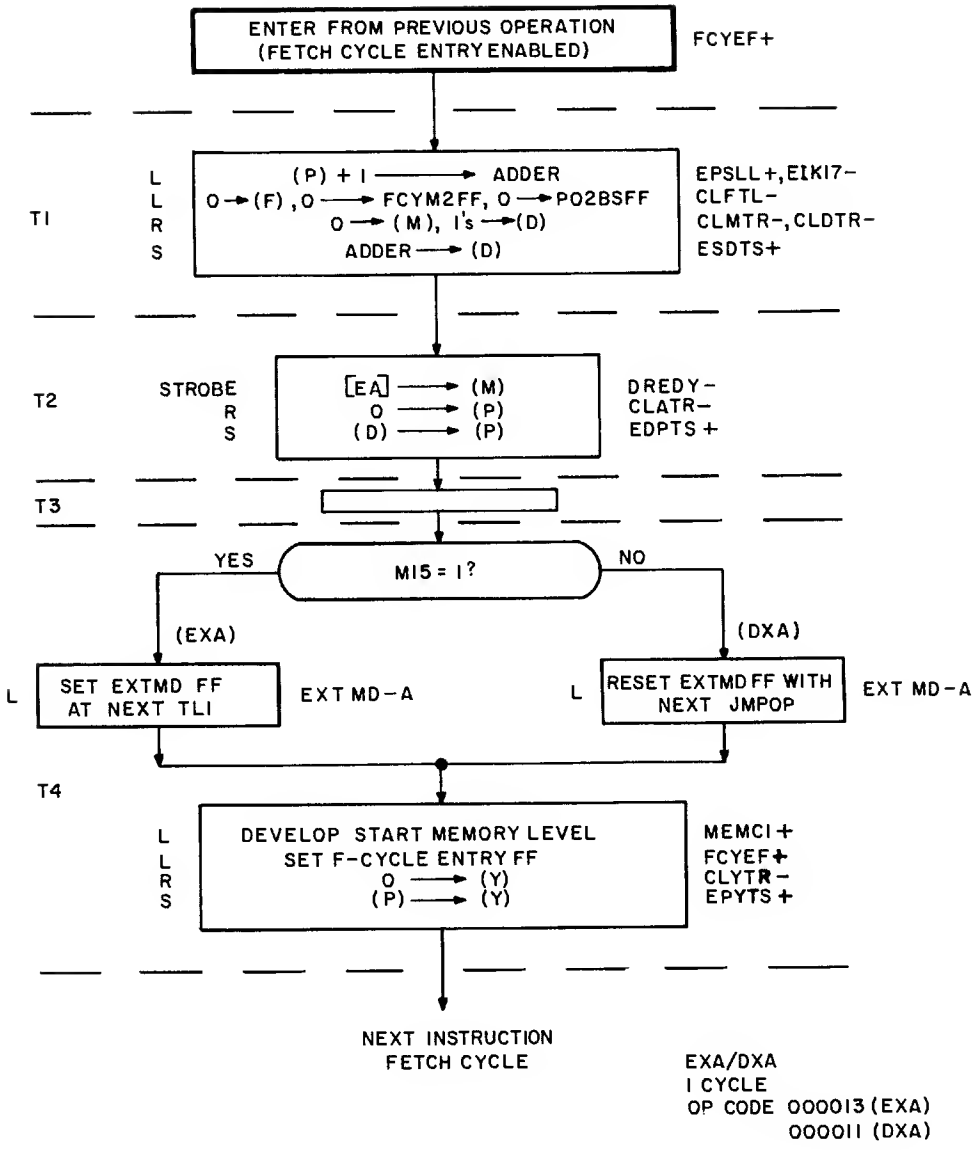
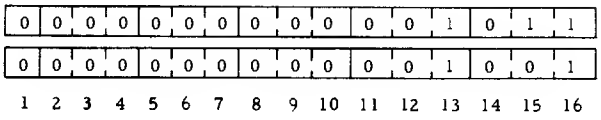


Figure 4. Memory Expansion Detailed Flow Chart

Table 3.
Memory Expansion Analysis

Instruction: Enable Extended Addressing (EXA)
Disable Extended Addressing (DXA)

Op Code: 000013 (EXA)
000011 (DXA) Type G, 1 cycle



Description: EXA places computer in extend mode.
DXA restores computer to normal mode.

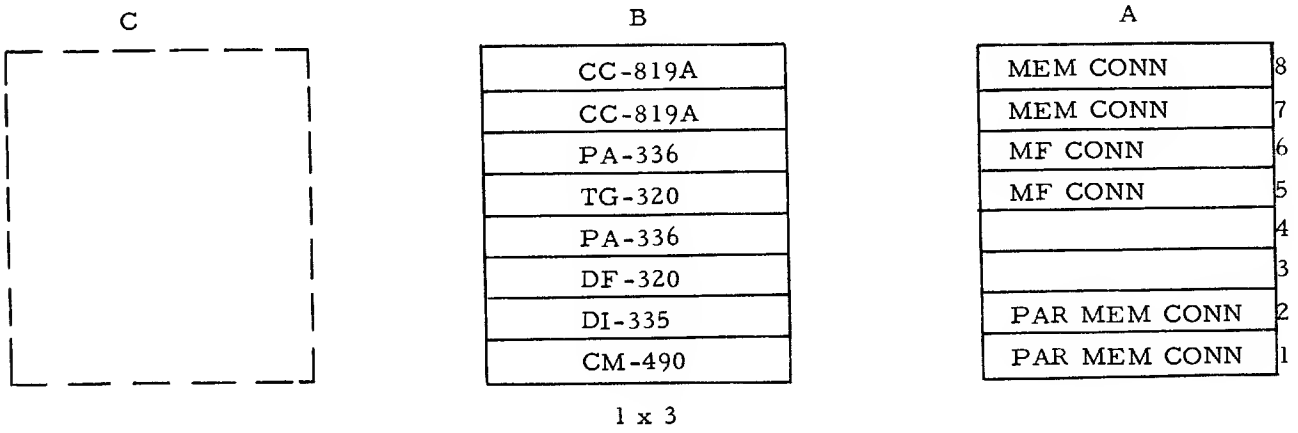
Execution Time (μs): 0.96

Signal	Origin	Cyc	Time	Clk	Signal Component	Origin	Destination	Operation Description
EPSLL+	128-K4	F	TLATE-	L	(FCYEF+)(TLATE-)	128-G3	101-116 A9	Enable P-register to adder
EIK17-	127-D5	F	TLATE-	L	(TLATE+)	127-K6	116 F7-F9 117 A1	Force carry to adder
CLFTL-	125-K8	F	TL1	L	(ICYEF-)(ACYEF-) (TL1FF+)	125-A6	120-A1 121-A5 125-D8 124-N6 124-N8	Clear F-register Clear shift counter Clear AZZZZ flip-flop Clear MAD flip-flop Clear DOC flip-flop
CLMTR-	128-D9	F	TL1	R	(MCRST+)(HOLDM-) (TL1FF+)	128-P9	101-116 L9 136-B8 136-B10	Clear M-register Clear M01FFB Clear M02FFB
CLDTR-	125-K5	F	TL1	R	(ICYEF-)(ACYEF+) (TL1FF+)(MCRST+)	125-A6	101-116 F11	Clear D-register to ONEs
ESDTS+	125-M4	F	TL1	S	(ICYEF-)(ACYEF+) (TL1FF+)(MCSET+)	125-A5	101-116 F5, F9	Enable adder sum to D-register
DREDY-	000-L2		T2		(MXTM6+)(WRITE-)	000-K2	008/007	Memory data set into M-register
CLPTR-	129-M10	F	TL2	R	(FCYEF+)(TL2FF+) (SCZR0+)(MEMAC-) (MCRST+)	129-E7/ L10 L10	101-116 L12	Clear P-register
EDPTS+	129-P9	F	TL2	S	(FCYEF+)(TL2FF+) (SCZR0+)(MEMAC-) (MCSET+)	129-L10	101-116 J11	Enable D-register to P-register
SEXTF+	136-G2	F	TL4	L	(GEN0B+)(TL4FF+) (M13FF+)(M15FF+) (MCSET+)	136-B3/ D4 136-M2	136-H2	Enable set EXTMD flip-flop at next TL1 Enable set PMIND flip-flop
SEXTF-	136-G2	F	TL4	L	(GEN0B+)(TL4FF+) (M13FF+)(M15FF-) (MCSET+)	136-B3/ D4	136-H2	Enable reset EXTMD flip-flop when next JMP is executed
							136-M2	Enable reset PMIND flip-flop
MEMC1+	126-K12	F	TL1	L	(TL1FF+)(SPM0D-) (IGACY-)	126-F12	150-A2	Enable start memory cycle
CLYTR-	129-P3	F	TL4	R	(SCZR0+)(TL4FF+) (MCRST+)	129-E2	101-116N12	Clear Y-register
EPYTS+	129-P4	F	TL4	S	(PISEX-)(EOINS+) (TL4FF+)(OPGJS-) (MCSET+)	129-E4	101-116 K11	Enable P-register to Y-register

PARTS LIST

Information not covered in the option parts complement (Table 4), including coding drawings, can be found in Chapter III of the H316 Circuit Modules and Parts Manual, Document No. 70130072166A.

The reference designation prefix "XX" indicates that the device is relocatable within the mainframe or either of the option drawers. Refer to Reference Designation Coding of Electronic Systems in the Honeywell Standard Practice Instruction, No. 125099023, for a detailed explanation of the Honeywell reference designations system. Final system configuration and locations of all option controllers will be determined by a System Release Notice. (See Figure 5 for memory expansion PAC layout.)



Note: CC-510A is located in logic mainframe

Figure 5. Memory Expansion PAC Layout

Table 4.
Option Parts Complement

Fig. No.	Designation	Part No.	Description	Qty. per Assy.
5	XX	70023577	Memory Expansion (Applicable to more than 16K)	REF
	XXB101	CM-490	TIMING DISTRIBUTION PAC (Refer to Appendix for parts breakdown.)	1
	XXB107, 08	CC-819A	DATA REGISTER PAC (Refer to Appendix for parts breakdown.)	2
	XXB102	DI-335	NAND TYPE 1 PAC (Refer to μ-PAC Instruction Manual, Vol. I, Section 3, Document No. 130071369 for parts breakdown.)	1
	XXB103	DF-320	NAND TYPE 2 PAC (Refer to μ-PAC Instruction Manual, Vol. 1, Section 10, Document No. 130071369 for parts breakdown.)	1
	XXB104, 06	PA-336	POWER AMPLIFIER PAC (Refer to μ-PAC Instruction Manual, Vol. 1, Section 6, Document No. 130071369 for parts breakdown.)	2
	XXB105	TG-320	TRANSFER GATE PAC (Refer to μ-PAC Instruction Manual, Vol. I, Section 10, Document No. 130071369 for parts breakdown.)	1
	A1AA15	CC-510A	EXTENDED ADDRESS MODULE (Refer to Appendix for parts breakdown.)	1
	XXAX06, 05 to A1BA18, 19	A013826 707	CABLE ASSEMBLY, SPECIAL PURPOSE μ-PAC to μ-PAC, 6 ft. overall length. (Refer to Document No. 70130072166, Chapter 111, Figure 3-13 for similar parts breakdown.)	2
	XXAX07, 08 to XXAX02, 01	A014998 702	CABLE ASSEMBLY, SPECIAL PURPOSE μ-PAC to μ-PAC, 7" flex jumper	2

CABLING

Figure 6 illustrates and defines cabling for the memory expansion option.

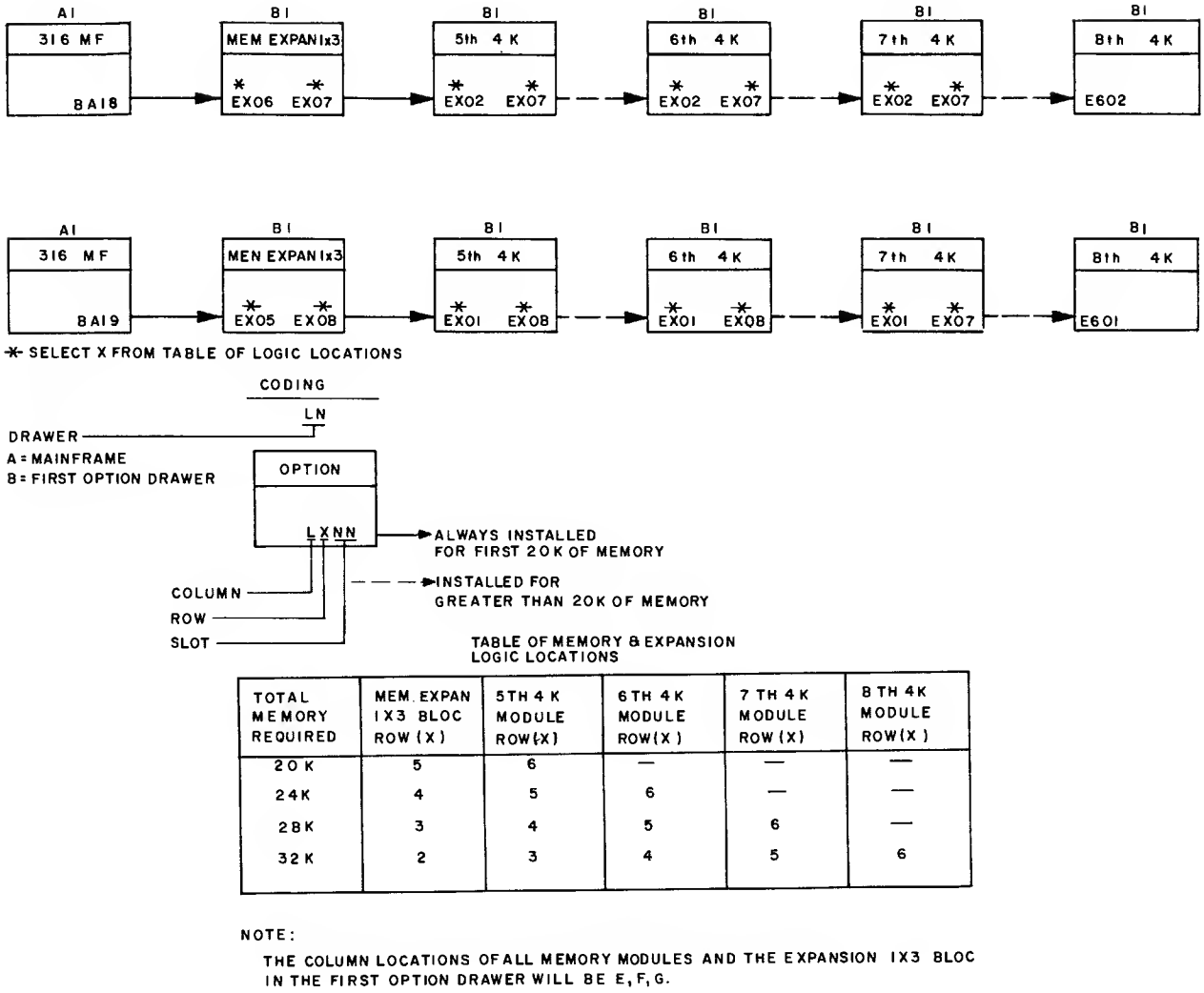


TABLE OF MEMORY & EXPANSION LOGIC LOCATIONS

TOTAL MEMORY REQUIRED	MEM EXPAN 1X3 BLOC ROW (X)	5TH 4K MODULE ROW(X)	6TH 4K MODULE ROW(X)	7TH 4K MODULE ROW (X)	8TH 4K MODULE ROW(X)
20K	5	6	—	—	—
24K	4	5	6	—	—
28K	3	4	5	6	—
32K	2	3	4	5	6

NOTE:

THE COLUMN LOCATIONS OF ALL MEMORY MODULES AND THE EXPANSION 1X3 BLOC IN THE FIRST OPTION DRAWER WILL BE E, F, G.

Figure 6. Cabling Chart

LOGIC BLOCK DIAGRAMS

The logic block diagrams for the Memory Expansion option are as follows:

LBD No.	Description	Dwg No.
0.000	H316 Memory Expansion Memory Timing and Control	70025825
0.001	H316 Memory Expansion Address Gating and Data Register Bits 1-5	70025828
0.002	H316 Memory Expansion Data Register Bits 6-14	70025834
0.003	H316 Memory Expansion Data Register Bits 15, 16 and Bank Signals	70025827
0.004	H316 Memory Expansion CP and Memory Connectors	70025831
0.005	H316 Memory Expansion 1x3 PAC-LOC	70025826
0.006	H316 Memory Expansion Address and Control	70025833
0.007	H316 Memory Expansion Memory Data	70025830
0.008	H316 Memory Expansion CP Connectors	70025832
0.136	H316 Memory Expansion Control Logic	70025829

L.B.D. NO. 0.000

JUMPERS FOR CM-490	
FROM	TO
MI-8	PIN 9
M2-1	C1B
M2-2, M3-6, M5-1	C32
M2-14	PIN 7
M2-7	C11
M3-6, M6-7	PIN 8
M3-7	C24
M4-1	C26
M4-2	PIN 26
M4-14	PIN 11
M4-7	C4
M4-8, M5-14	C15
M5-2	PIN 20
M6-2	C26
C25	PIN 10
M5-8	C23

▲ SOLDER TO ETCH

NOTES:

⚠ SOURCE FOR SIGNAL PLOAD- IS MEMORY PARITY WHEN INSTALLED

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REVISIONS	REV.		
	A	S. R. 54-3915	
	B	ECO 8538 EXT. CHGS SEE ECO A.K. 7/2/70	
	C	ECO 9490 EXT. CHGS SEE ECO A.K. 6/4/71	
	D	ECO 20687 CHG'D PER ECO T.L.B. 12/14/72	
	E	ECO 3062 SEE ECO T.L.B. 73/5/9	

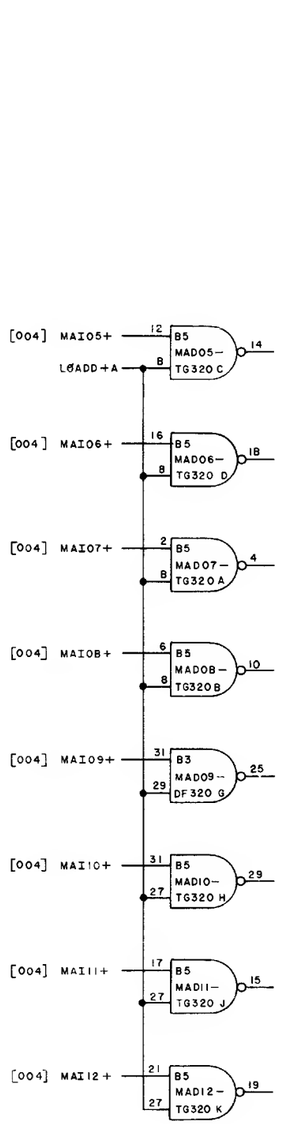
HONEYWELL INC
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham Mass

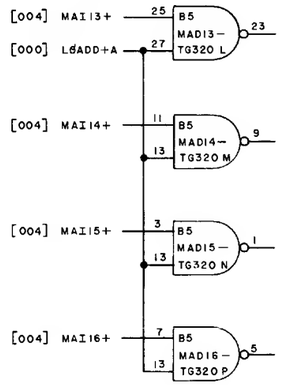
DR. D HAMEL	DATE
ENG. R. ALBRIGHT	5/15/69
APP.	9/12/69
PROJECT NO. 53217	

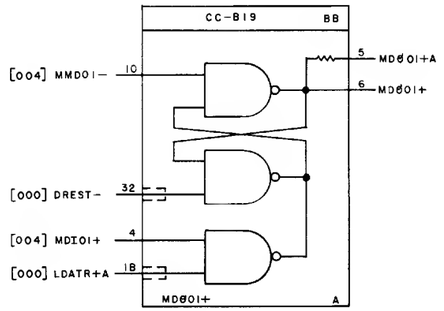
TITLE
H-316
MEMORY EXPANSION
MEMORY TIMING & CONTROL

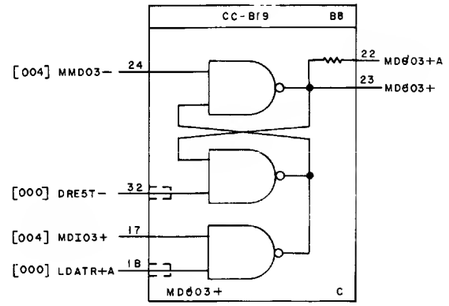
SIZE C | DWG NO. 70025825 | REV. E

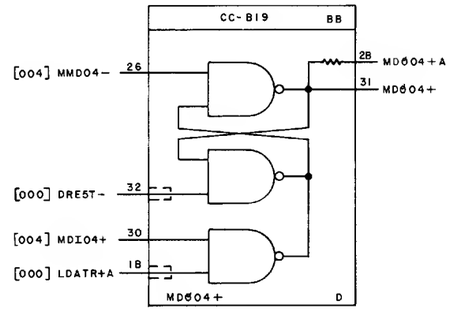
L.B.D. NO. 0.001











NOTES:

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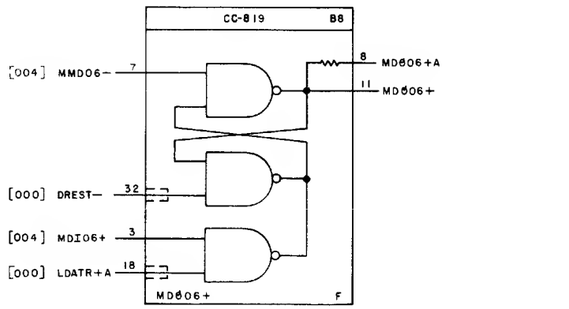
REV.	REVISIONS	CHK
A	S.R. 54-3915	
B	ECO 8458 EXT. CHGS SEE ECO 3/27/70 A.K.	
C	ECO 9617 SEE ECO SSR 7/2/71	
D	ECO 20687 SEE ECO 12/13/72 T.L.B.	

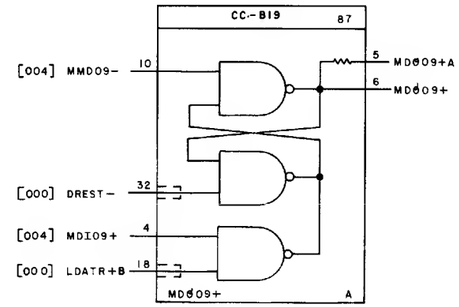
HONEYWELL INC
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham Mass

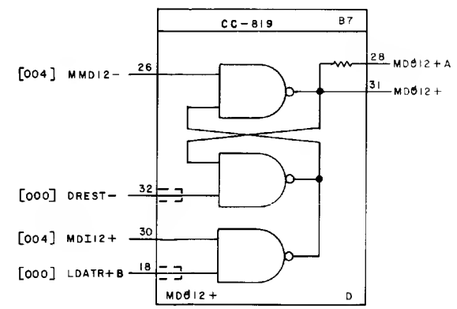
DR. D HAMEL	DATE
ENG. R. ALBRIGHT	5/13/69
APP.	9/12/69
PROJECT NO. 53217	

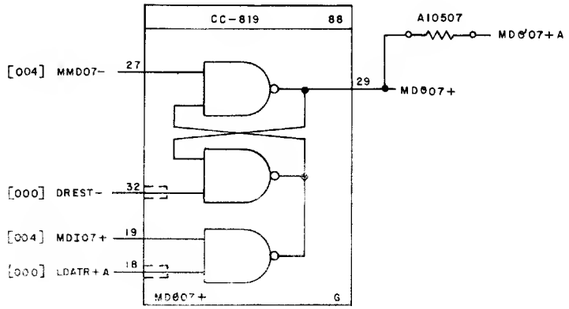
TITLE
H-316
MEMORY EXPANSION
ADDRESS GATING & DATA
REGISTER BITS 1-5

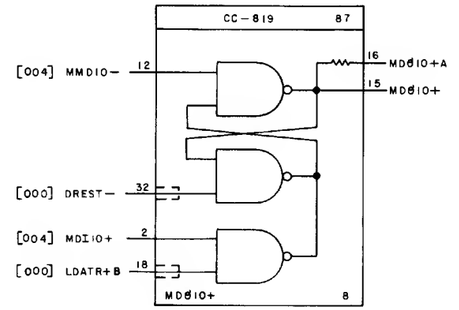
SIZE C | DWG NO. 70025828 | REV. D

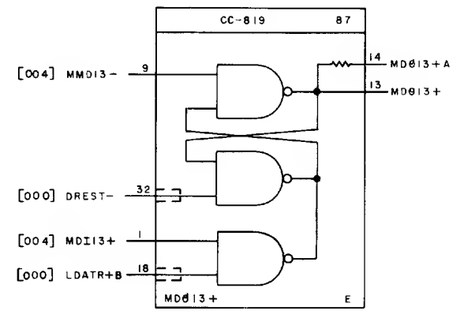


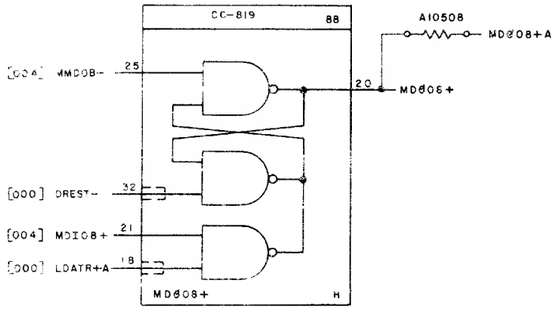


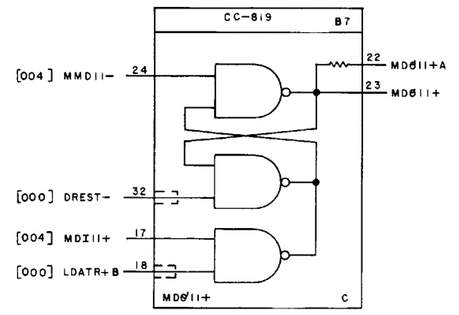


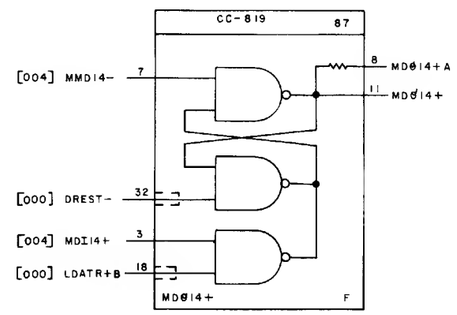












NOTES:

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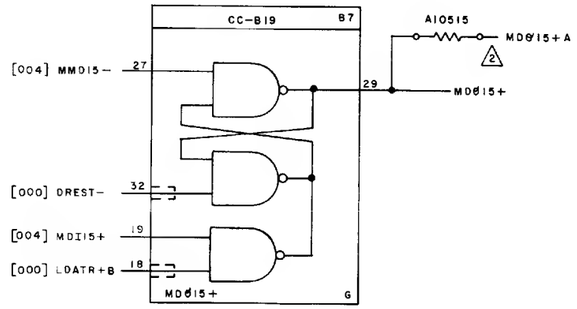
REVISIONS	REV.		
	A	SR. 54-3915	
	B	ECO 8458 EXT. CHGS SEE ECO 3/27/70 A.K.	
	C	ECO 9490 EXT. CHGS SEE ECO 6/4/71 A.K.	
	D	ECO 9617 SEE ECO 7/2/71 SSR	
	E	ECO 20687 SEE ECO 12/14/72 T.L.B.	

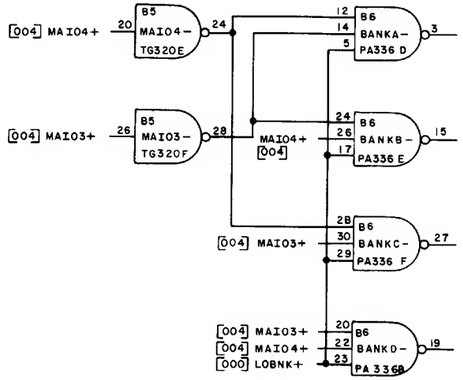
HONEYWELL INC
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham Mass

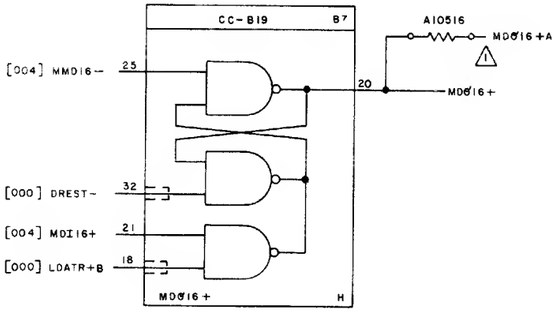
DR. D HAMEL	DATE
ENG. R. ALBRIGHT	5/13/69
APP.	
PROJECT NO. 53217	

TITLE
H-316-0602
MEMORY EXPANSION
DATA REGISTER BITS 6-14

SIZE C | DWG NO. 70025834 | REV. E







NOTES:

1. ADD A RESISTOR FROM BI0720 TO AI0516 ON THE BACKPLANE
2. ADD A RESISTOR FROM BI0729 TO AI0515 ON THE BACKPLANE

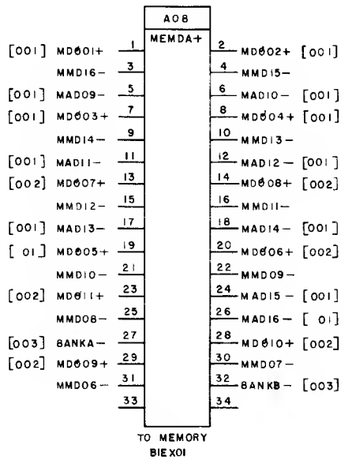
REV.	REVISIONS	CHK
A	S.R. 54-3915	
B	ECO 8458 EXT. CHGS SEE ECO 3/27/70 A.K.	
C	ECO 9490 EXT. CHGS SEE ECO 6/4/71 A.K.	
D	ECO 9617 SEE ECO 7/2/71 SSR	
E	ECO 20687 SEE ECO 12/13/72 12/27 T.L.B.	

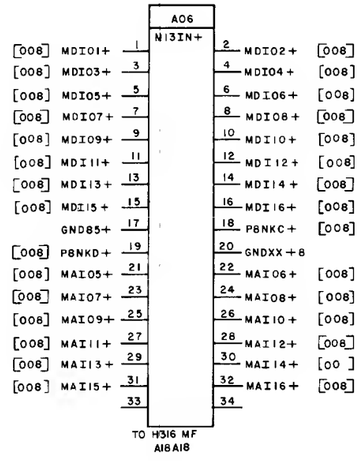
HONEYWELL INC
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham Mass

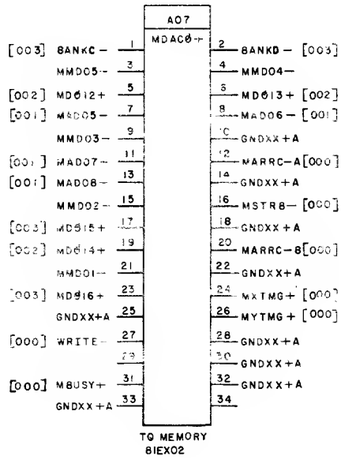
DR. D. HAMEL	DATE
ENG. R. ALBRIGHT	5/13/69
APP.	9/12/69
PROJECT NO. 53217	

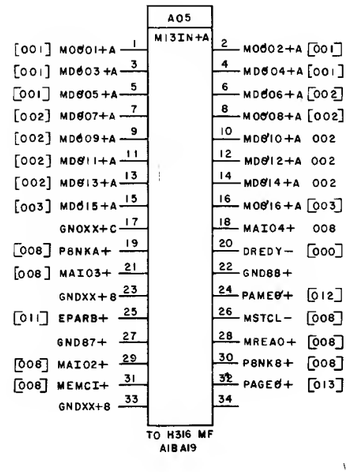
TITLE
H-316-0602
MEMORY EXPANSION
DATA REGISTER BITS 15,16
& BANK SIGNALS

SIZE C | DWG NO. 70025827 | REV









NOTES:
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REV.	REVISIONS	CHK
A	S.R. 54-3915	
B	ECO 20687 SEE ECO 12/13/72 T.L.B.	

HONEYWELL INC
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham Mass

DR. D. HAMEL	DATE
ENG. R. ALBRIGHT	5/15/69
APP.	9/12/69
PROJECT NO. 53217	

TITLE
H-316
MEMORY EXPANSION
C.P. & MEMORY CONN.

SIZE C | DWG NO. 70025831 | REV. B

A B C D E F G H J K L

LBD. NO.
0.005

4

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8															
7															
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5															
4															
3															
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1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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4															
3															
2															
1															

3

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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2															
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LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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4															
3															
2															
1															

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
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7															
6															
5															
4															
3															
2															
1															

1

C

	LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
	8															
	7															
△1	6	PG-340	13	13												
	5															
	4	DI-335	11	11	11	12	12	12	12	00	00	00				
△1	3	CC-559A	12													
△1	2	CC-559A	11													
△1	1	DI-335	13	13	13	13	13	13	13	13	11	11				

B

LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	CC-819A	01	01	01	01	01	02	02	02						
7	CC-819A	02	02	02	02	02	02	03	03						
6	PA-336	00	03	00	03	03	03								
5	TG-320	01	01	01	01	03	03		01	01	01	01	01	01	01
4	PA-336	00	00	00	00	11	00								
3	DF-320	00	00	00		00	00	01	03						
2	DI-335	00	00	00	00	00	00	00	00	00	00				
1	CM-490	00													

A

	LOC	PAC	A	B	C	D	E	F	G	H	J	K	L	M	N	P
	8			CONN. MEMORY INTERFACE												
	7			CONN. MEMORY INTERFACE												
	6			CONN. C.P. INTERFACE												
	5			CONN. C.P. INTERFACE												
	4															
	3															
△1	2			CONN PAR MEM INTERFACE												
△1	1			CONN PAR. MEM INTERFACE												

1 2 3 4 5 6 7 8 9 10 11

NOTES:

△1 ADDED FOR MEMORY PARITY OPTION.

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REV	REVISIONS	CHK
A	SR, 5A-3915	
B	ECO 8300 CC-559A WAS CC-559	
C	ECO 9617 SEE ECO 7/2/71 SSR	
D	ECO 20687 SEE ECO 12/14/72 12/27 T.L.B.	

–	–	P70025826	PARTS LIST

HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path, Framingham, Mass

DR. A. KMICINSKI	DATE 8/6/69
ENG. R. ALBRIGHT	
APP. G. B. [signature]	9/12/69
PROJECT NO. 53217	

TITLE
PAC COMP/ALLOC
MEMORY EXPANSION
1 X 3

SIZE	DWG NO.	REV.
C	70025826	D

L.B.D. NO. 0.006

[103] Y03FF– A9 — A15 M03AD+ 510 67 — 62Ω — A3

[104] Y04FF– A10 — A15 M04AD+ 510 68 — 62Ω — A5

[105] Y05FF– A18 — A15 M05AD+ 510 69 — 62Ω — A21

[106] Y06FF– A20 — A15 M06AD+ 510 70 — 62Ω — A23

[107] Y07FF– A38 — A15 M07AD+ 510 71 — 62Ω — A35

[108] Y08FF– A40 — A15 M08AD+ 510 72 — 62Ω — A37

[109] Y09FF– B10 — A15 MD9AD+ 510 73 — 62Ω — B5

[110] Y10FF– B27 — A15 M10AD+ 510 75 — 62Ω — B23

[111] Y11FF– B30 — A15 M11AD+ 510 76 — 62Ω — B25

[112] Y12FF– B45 — A15 M12AD+ 510 77 — 62Ω — B43

[113] Y13FF– B48 — A15 M13AD+ 510 78 — B2Ω — B44

[114] Y14FF– C12 — A15 M14AD+ 510 79 — 62Ω — C10

[115] Y15FF– C11 — A15 M15AD+ 510 80 — 62Ω — C9

[116] Y16FF– B11 — A15 M16AD+ 510 61 — 62Ω — B7

[136] EXTMD-A
[142] ENTRP– B26 — A15 EXTRP+ 510 83 — [102] D02FF+ B24 — A15 EXD02– 510 64 — A15 BSD02+ 510 91 — B8

[136] P02BS+
[136] EXTMD-A — A15 EXP02– 510 85

[134] BREAK+ A41
[119] ICYEF+ B14
[118] TLIFF+A A44
— A15 BRICY– 510 97

[136] Y02FF+
[136] EXTMD+ — A15 EXY02+ 510 — A15 YNODE–A 510 — B15

[102] Y02FF– A28 — A15 M02AD+ 510 — 62Ω — B13

[136] ACYEF+
[120] JSTØP+ B03
[136] EXTMD–A — A15 BSH02– 510 — A19

IØGRP+ A45
[136] ACYEF+ — A15 IGACE+ 510 B6 — [118] TLIFF+A A44 / [135] SPM0D– A27 — A15 MMCYI– 510 B7

[126] RRCXX– A42 — A15 MREAD+ 510 92 — C26

[42] DMCCI– C27 — A15 MMCYI+ 510 94 — MMCYI+ — A31

[136] Y02FF+ — A15 MEMCI+A 510 88 — A29 — MEMCI+

NOTES:

REVISIONS	REV.			
CHK		SR. 54-3915	ECO 20687	B
			SEE ECO 12/14/72	A7 T.L.B

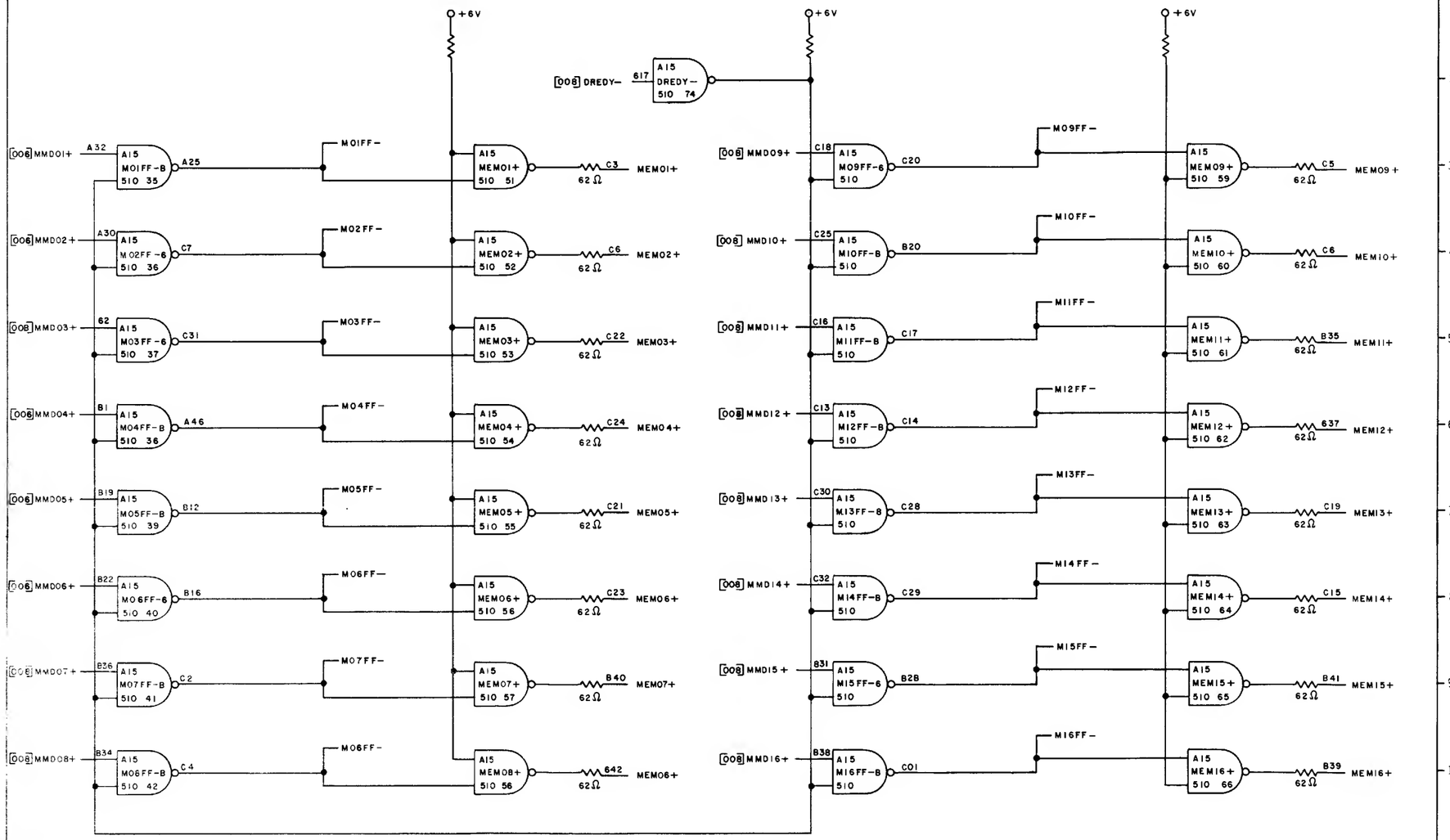
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham Mass

DR. D HAMEL	DATE
ENG. R. ALBRIGHT	5/16/69
APP.	9/12/69
PROJECT NO. 53217	

TITLE
H-316
MEMORY EXPANSION/PARITY
ADDRESS AND CONTROL

SIZE C | DWG NO. 70025833 | REV. B

L.B.D. NO. 0.007



NOTES:

REV	REVISIONS	CHK
A	S.R. 58-3915	
B	ECO 20687 SEE ECO 12/14/72 T.L.B.	

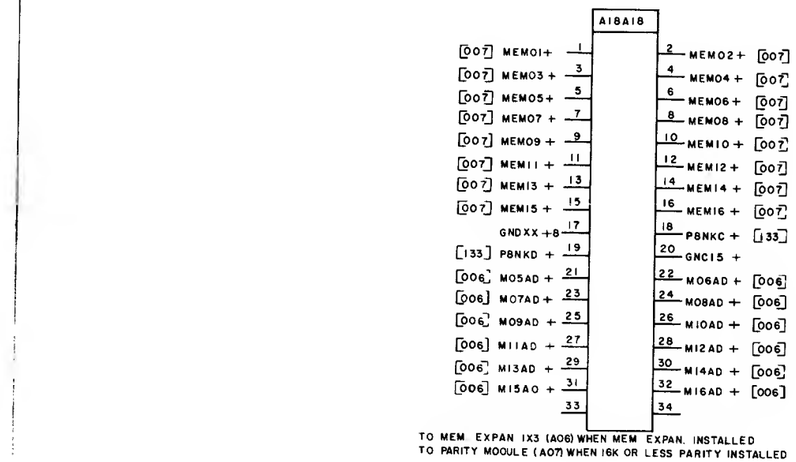
HONEYWELL INC.
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham Mass

DR. D HAMEL	DATE
ENG. R. ALBRIGHT	5/12/69
APP.	9/12/69
PROJECT NO. 53217	

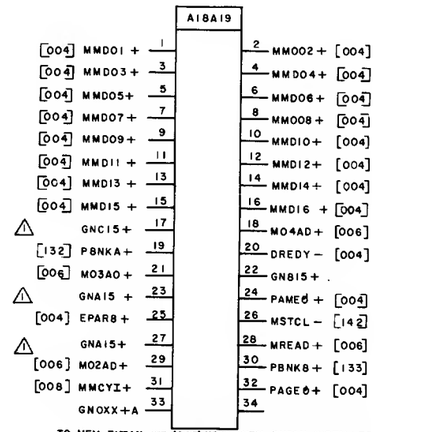
TITLE
H-316
MEMORY EXPANSION/PARITY
MEMORY DATA IN/OUT

SIZE C | DWG NO. 70025830 | REV. B

L.B.D. NO. 0.008



TO MEM. EXPAN 1X3 (A06) WHEN MEM EXPAN. INSTALLED
TO PARITY MOOULE (A07) WHEN 16K OR LESS PARITY INSTALLED



TO MEM. EXPAN. 1X3 (A05) WHEN MEM. EXPAN. INSTALLED
TO PARITY MODULE (A08) WHEN 16K OR LESS PARITY INSTALLED

NOTES:

⚠ SEE MAINFRAME COVER SHEET NOTES FOR WIRE CHANGES WHEN 16K OR LESS OF PARITY IS INSTALLED

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REV	REVISIONS	CHK
A	5.5K-3915	
B	ECO 20687 SEE ECO 12/15/72 T.L.B.	

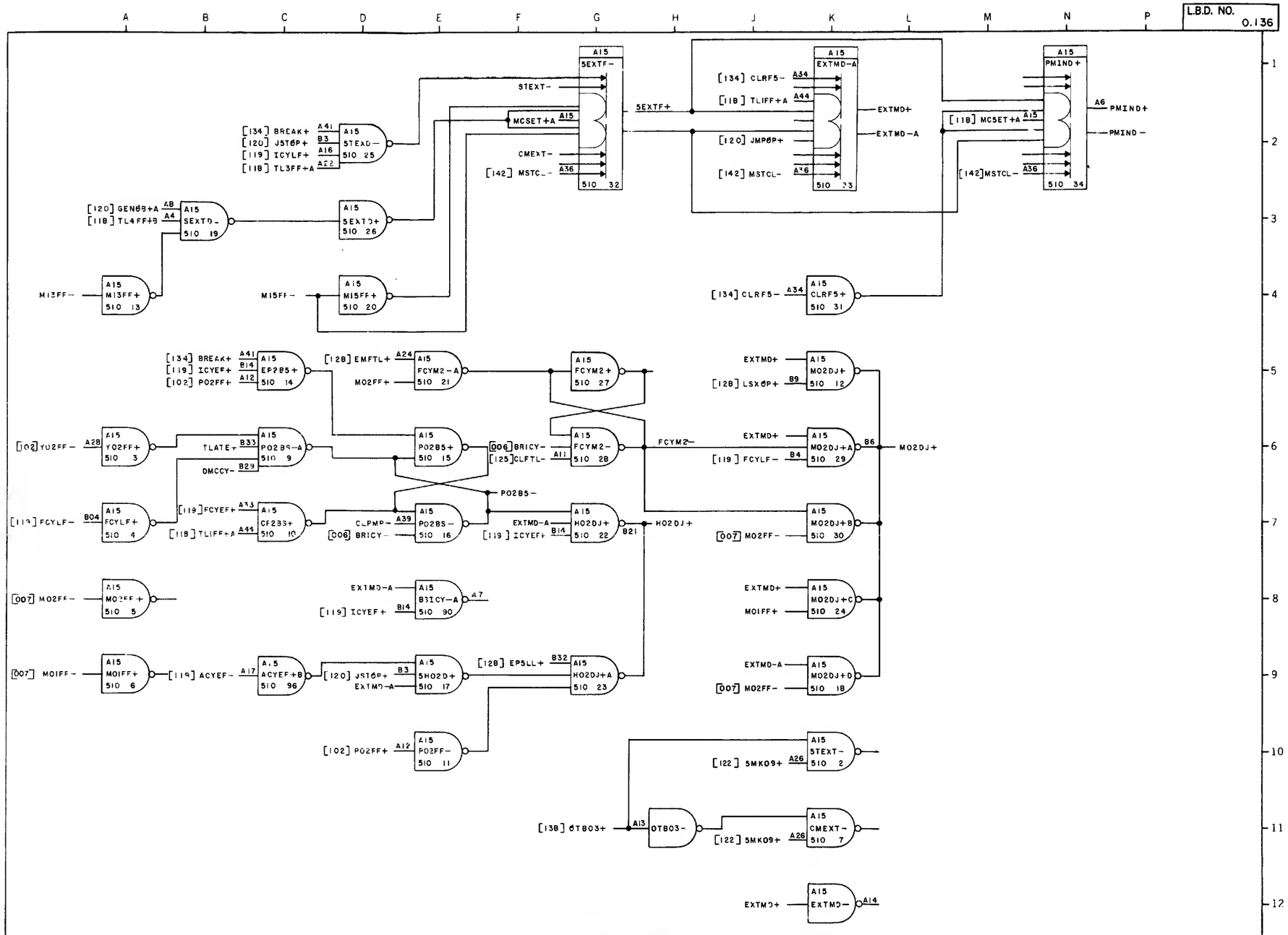
HONEYWELL INC
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham Mass

DR.	O. HAMEL	DATE
ENG.	R. ALBRIGHT	5/16/69
APP.		9/12/69
PROJECT NO.	53217	

TITLE
MEMORY EXPANSION/PARITY
C. P. CONNECTORS

SIZE C | DWG NO. 70025832 | REV. B

L.B.D. NO. 0.136



NOTES:

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REV	REVISIONS	CHK
A	S.R. 54-315	

HONEYWELL INC
COMPUTER CONTROL DIVISION
Old Connecticut Path Framingham Mass

DR. D. HAMEL	DATE
ENG. R. ALBRIGHT	5/16/69
APP.	
PROJECT NO. 53217	

TITLE
H-316
MEMORY EXPANSION
CONTROL LOGIC

SIZE C | DWG NO 70025829 | REV. A

APPENDIX
MODULE DESCRIPTIONS

This Appendix contains a description of the special μ-PAC and H316 Modules. The specifications for integrated circuit plug-in devices used on the CC-510A Extended Address Module are presented in Honeywell, Computer Control Division Document No. 70130072166 (M-494), Chapter I. The operation of this module is discussed in the Theory of Operation in this manual.

EXTENDED ADDRESS MODULE, MODEL CC-510A

Electrical Parts List

Ref. Desig.	Description	CCD Part No.
C1-C5	CAPACITOR, FIXED, DIELECTRIC: 0.033 µF ± 20%, 50 Vdc	70 930 313 016
CR1-CR4	DIODE, SILICON	70 943 083 002
M1, M7	MICROCIRCUIT: Type 937, hex inverter	70 950 105 011
M2, M38	MICROCIRCUIT: Type 949, quad NAND gate, integrated circuit	70 950 105 010
M3, M8, M41	MICROCIRCUIT: Type 963, triple NAND gate, integrated circuit	70 950 105 012
M4, M10	MICROCIRCUIT: Type SN7401, NAND gate, integrated circuit	70 950 100 032
M5, M6, M37	MICROCIRCUIT: Type 944, dual NAND gate, integrated circuit	70 950 105 008
M9	MICROCIRCUIT: Type 961, dual NAND gate, integrated circuit	70 950 105 009
M11, M12, M13	MICROCIRCUIT: Type F-04, flip-flop, integrated circuit	70 950 100 004
M14-M21	MICROCIRCUIT: Type F-01, NAND gate, integrated circuit	70 950 100 001
M22-M36, M39	MICROCIRCUIT: Type F-03, power amplifier, integrated circuit	70 950 100 003
M40	MICROCIRCUIT: Type F-02, quad NAND gate, integrated circuit	70 950 100 002
R1-R23, R25-R31, R34, R35	RESISTOR, FIXED, COMPOSITION: 62 ohms ± 5%, 1/4W	70 932 007 020
R24, R32, R33, R36	RESISTOR, FIXED, COMPOSITION: 1K ± 5%, 1/4W	70 932 007 049

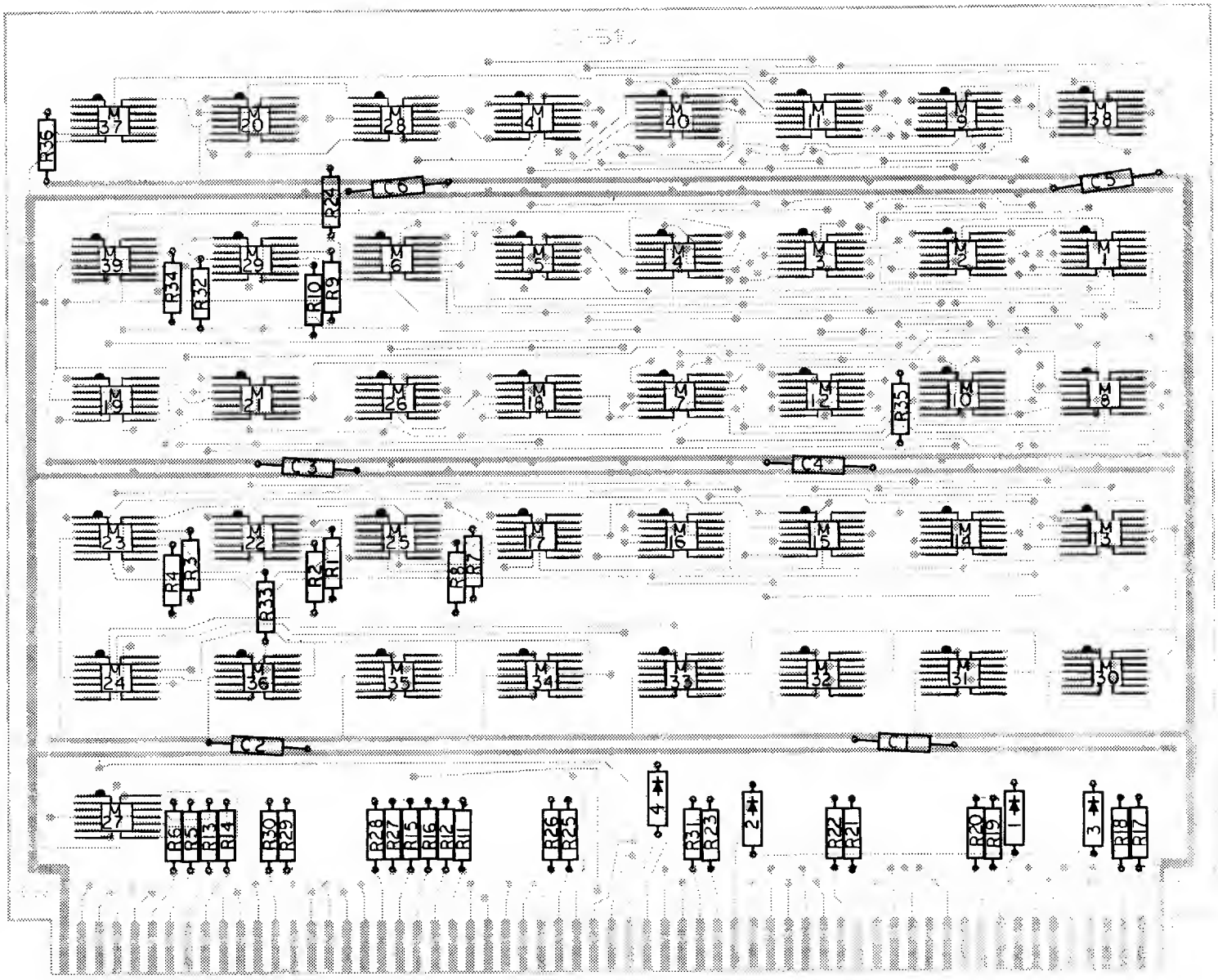
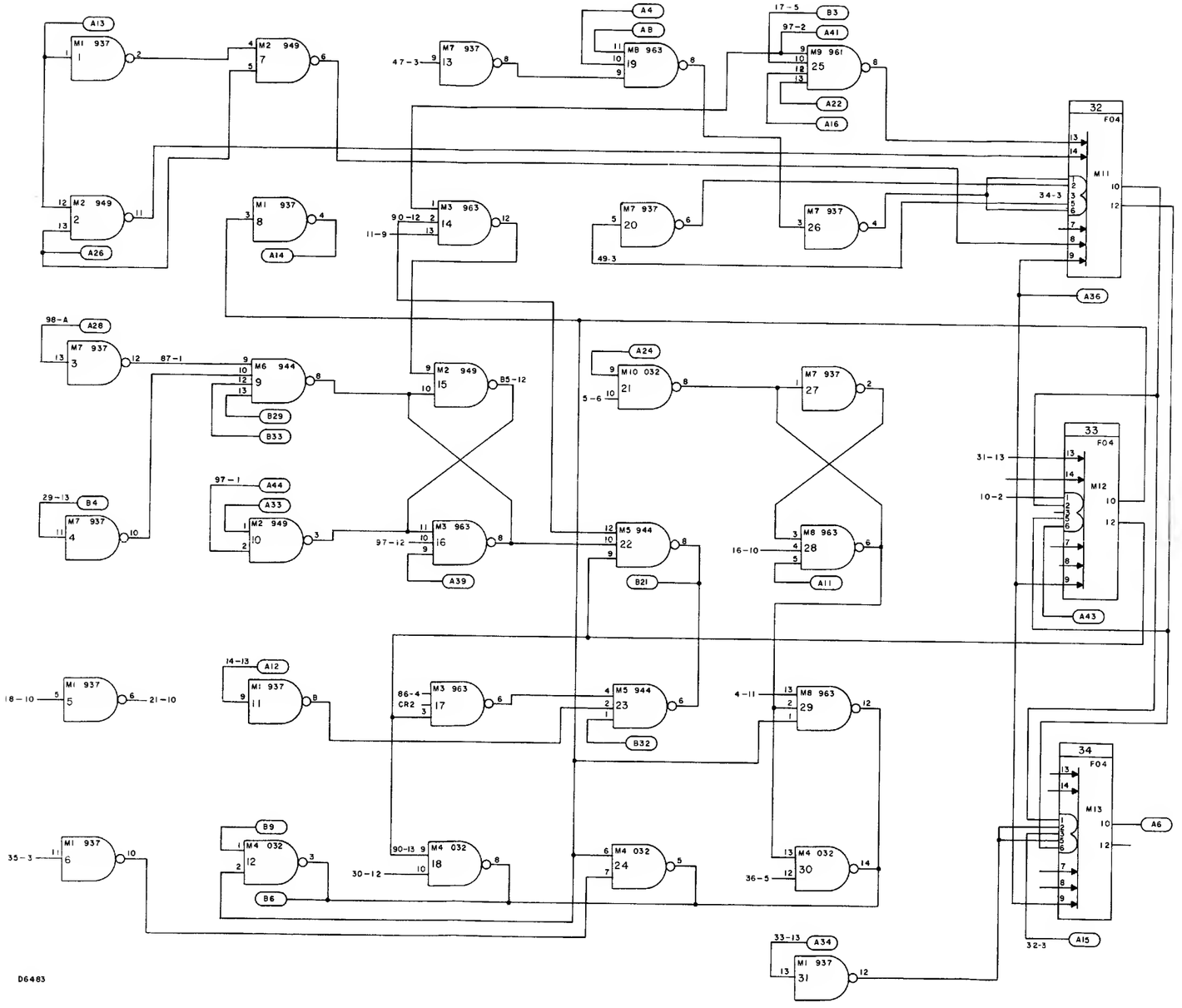


Figure CC-510A-1. Extended Address Module, Parts Location



M#	GRID CORD	TYPE	GATES 1	2	3	4	5	6
1		937	1	5	6	11	31	8
2		949	2	7	10	15		
3		963	14	16	17			
4		032	12	18	24	30		
5		944	22	23				
6		944	9	74				
7		937	3	4	13	20	26	27
8		963	19	28	29			
9		961	87	25				
10		032	88	21				
11		F04	32					
12		F04	33					
13		F04	34					
14		F01	35	36				
15		F01	37	38				
16		F01	39	40				
17		F01	41	42				
18		F01	49	50				
19		F01	47	48				
20		F01	45	46				
21		F01	43	44				
22		F03	51	52				
23		F03	53	54				
24		F03	55	56				
25		F03	57	58				
26		F03	65	66				
27		F03	63	64				
28		F03	61	62				
29		F03	59	60				
30		F03	67	68				
31		F03	69	70				
32		F03	71	72				
33		F03	73	81				
34		F03	75	76				
35		F03	77	78				
36		F03	79	80				
37		944	98					
38		949	86	90	96			
39		F03	92	94				
40		F02	83	84	85	91		
41		963	97	99				

TYPE	VCC	GRD
930 963	14	7
SN 7401	4	11
SHUL F23	4	10
F01 F03	4	11
F09	4	11

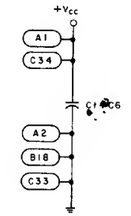


Figure CC-510A-2. Extended Address Module, Schematic Diagram (Sheet 1 of 2)

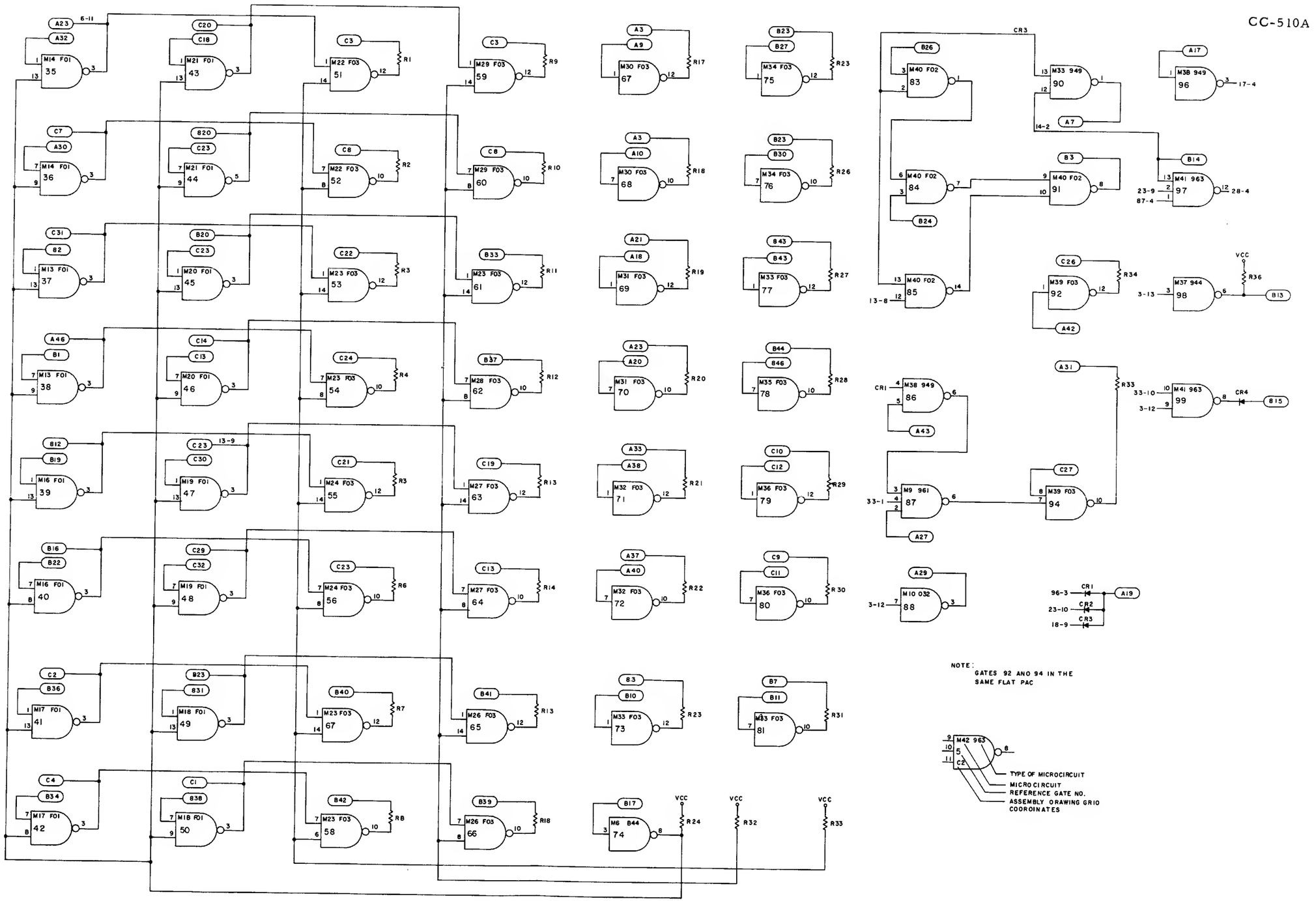


Figure CC-510A-2. Extended Address Module, Schematic Diagram (Sheet 2 of 2)

TIMING DISTRIBUTOR PAC, MODEL CM-490

The Timing Distributor PAC, Model CM-490 (Figures 1, 2, and 3), provides accurately timed pulse sequences for use in timing and control applications. The CM-490 contains one control flip-flop, a 288-ns-long delay line with 12-ns taps, a 96-ns-long delay line with 12-ns taps, and nine inverting power amplifier output circuits.

The PAC consists of two double-sided printed circuit boards sandwiched together for ease of mounting in a μ-BLOC. Board A, which plugs into the connector, contains the four delay lines (DL1 through DL4) and five F-03 microcircuit power amplifiers. The delay lines are positioned between the two circuit boards to expose the etched side of board A for timing jumper adjustment.

Board B contains an F-04 microcircuit flip-flop, discrete drivers, and termination loads.

NOTE

The CM-490 PAC occupies two slots in a taper-pin BLOC and three slots in a solderless-wrap BLOC, or the end slot (position) in either.

Circuit Function

Delay lines DL1 through DL2 can be tapped and jumpered to the output power amplifiers and the delay line, DL4, to provide accurately timed output pulses. Input connection points for each amplifier are located on the PAC to facilitate timing flexibility. Refer to Table 1 and Figure 3.

The dc reset of the flip-flop may also be tapped from any point along DL1 through DL3 to allow recirculation of the opposite driving edge, thereby establishing fixed pulse widths. An ac set, a dc reset, and the two outputs of the flip-flop are brought to the PAC connector.

Delay line DL4 and its associated output power amplifiers may be interconnected to provide inverted pulses with a 12-ns delay resolution.

Specifications

Input Loading

Flip-flop dc reset:	2/3 unit load
Flip-flop ac set:	1 unit load
Power amplifiers:	2 unit loads each

Circuit Delay

Flip-flop:

Set input to set output or reset input to reset output

65 ns (typ); 80 ns (max)

Set input to reset output or reset input to set output

45 ns (typ); 60 ns (max)

Power amplifiers:

24 ns (typ); 30 ns (max) each

Delay to first tap (C1):

60 ns (typ); 80 ns (max)

Output Drive Capability

Flip-flop set:	8 unit loads
Flip-flop reset:	4 unit loads
Power amplifiers:	25 unit loads each

Delay Line (DL1 through DL3)

Length: 288 ns ±5%, 24 taps, each 12 ±1 ns
Minimum pulse width: 85 ns
Maximum pulse width: 330 ns

Delay Line (DL4)

Length: 96 ns ±5%, 8 taps, each 12 ±1 ns

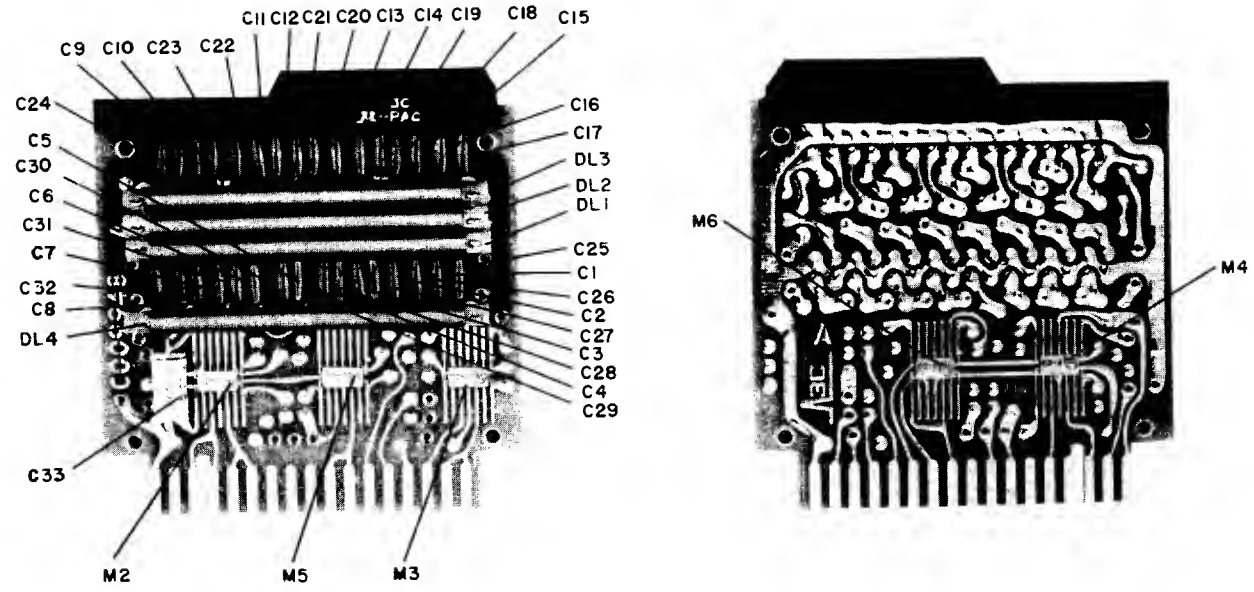
Current Requirements

+6V: 175 mA
-6V: 100 mA

Power Dissipation

1.10W (max)

Board A (B70010795, Rev. F)



Board B (B70010796, Rev. D)

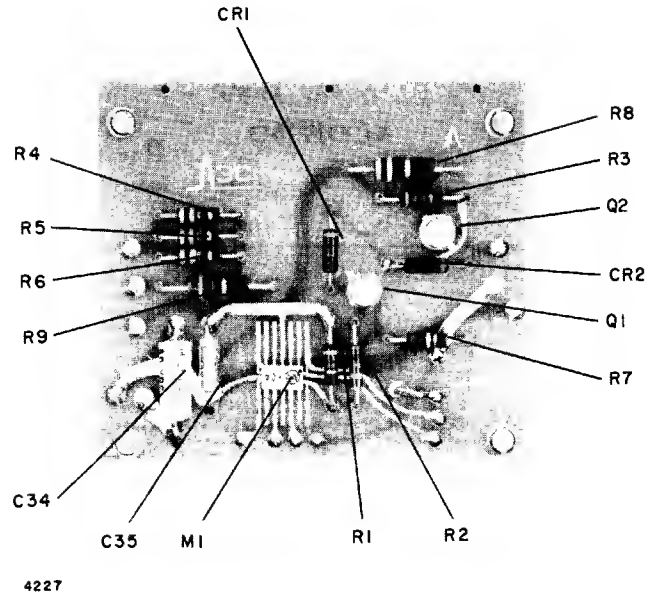
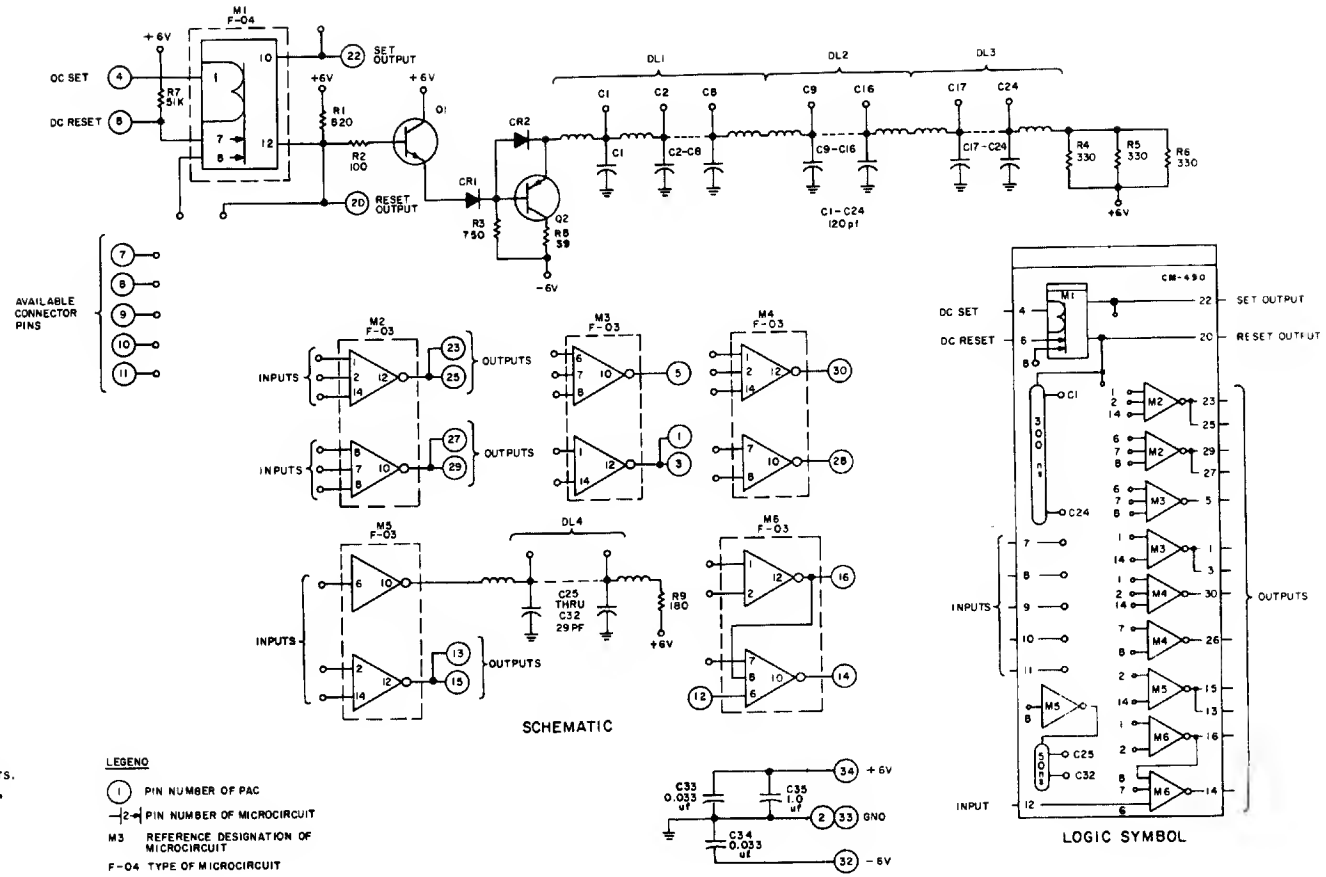


Figure 1. Timing Distributor PAC, Model CM-490, Parts Locations

ELECTRICAL PARTS LIST (No. P70010795, Rev. F, and P70010796, Rev. D)

Reference Designation	Description	CCD Part No.
C1-C32	CAPACITOR, FIXED, MICA DIELECTRIC: 120 pF ±2%, 100 Vdc	930 004 219
C33, C34	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 μF ±20%, 50 Vdc	930 313 016
C35	CAPACITOR, FIXED, TANTALUM ELECTROLYTIC: 1.0 μF ±20%, 35 Vdc	930 217 015
CR1, CR2	DIODE	943 088 001
DL1-DL4	COIL, DELAY LINE	B000 206 703
M1	MICROCIRCUIT: F-04, flip-flop integrated circuit	950 100 004
M2-M6	MICROCIRCUIT: F-03, power amplifier integrated circuit	950 100 003
Q1	TRANSISTOR: Replacement Type 2N3011	943 722 002
Q2	TRANSISTOR: Replacement Type 2N3012	943 721 002
R1	RESISTOR, FIXED, COMPOSITION: 820 ohms ±5%, ¼W	932 007 047
R2	RESISTOR, FIXED, COMPOSITION: 100 ohms ±5%, ¼W	932 007 025
R3	RESISTOR, FIXED, COMPOSITION: 750 ohms ±5%, ¼W	932 007 046
R4-R6	RESISTOR, FIXED, COMPOSITION: 330 ohms ±5%, ¼W	932 007 037
R7	RESISTOR, FIXED, COMPOSITION: 51K ±5%, ¼W	932 007 090
R8	RESISTOR, FIXED, COMPOSITION: 39 ohms ±5%, ½W	932 004 015
R9	RESISTOR, FIXED, COMPOSITION: 180 ohms ±5%, ½W	932 004 031



NOTES

TAP DESIGNATIONS REFER TO CIRCUIT COMPONENTS.
EXAMPLE: C1 TO TAP AT C1; M3-8 TO TAP AT M-S, PIN 8, 10 TO TAP AT PIN 10 OF PAC.

REFER TO TABLE I FOR DELAY LINE DELAYS IN NANOSECONGS.

B3121A

LEGEND

(1) PIN NUMBER OF PAC

→2← PIN NUMBER OF MICROCIRCUIT

M3 REFERENCE DESIGNATION OF MICROCIRCUIT

F-04 TYPE OF MICROCIRCUIT

Figure 2. Timing Distributor PAC, Model CM-490, Schematic Diagram and Logic Symbol (Dwg B70010797, Rev. E)

TABLE 1
DELAY LINE TAP POINTS WITH CORRESPONDING DELAY LINE DELAYS
(Refer to Figure 2)

Delay Line Jumper Connection	Delay Line Delay (ns)	Delay Line Jumper Connection	Delay Line Delay (ns)
C1	12	C19	228
C2	24	C20	240
C3	36	C21	252
C4	48	C22	264
C5	60	C23	276
C6	72	C24	288
C7	84		
C8	96		
C9	108		
C10	120		
C11	132	C25	12
C12	144	C26	24
C13	156	C27	36
C14	168	C28	48
C15	180	C29	60
C16	192	C30	72
C17	204	C31	84
C18	216	C32	96

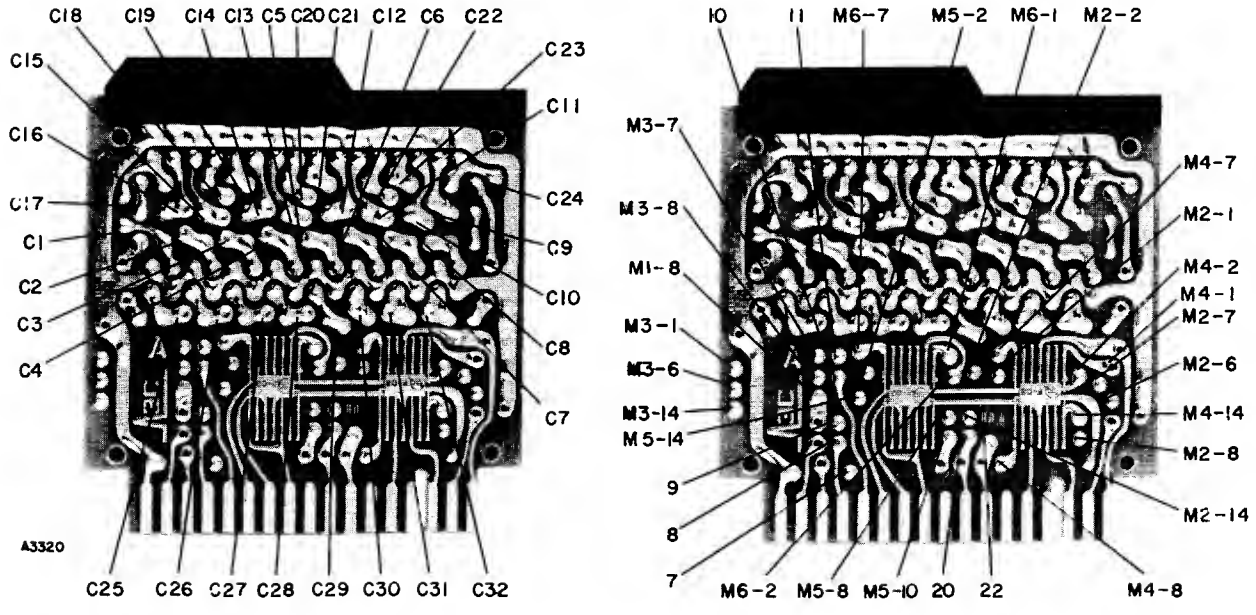


Figure 3. Timing Distributor PAC, Model CM-490, Delay Line Timing

DATA REGISTER PAC, MODELS CM-493/CC-819A

The Data Register PAC, Models CM-493/CC-819A (Figures 1 and 2), consists of eight register stages, each containing a power amplifier stage. Each stage has a separate set input and data input with reset and data strobe inputs common to all stages. Direct outputs are available on all stages while series-terminated outputs are available on two stages. The power amplifiers have the capability of driving twisted pair cables up to six feet in length.

SPECIFICATIONS

Frequency of Operation

DC to 5 MHz

Current Requirements

+6V: 210 mA (max)

Set Input Pulse Width

70 ns neg (min)

Reset Input Pulse Width

80 ns neg (min)

Data and Strobe Coincidence

70 ns (min)

Circuit Delay

Set Input to Output

$\leq$ 40 ns

Reset Input to Output

$\leq$80 ns

Data or Strobe Input to Output

$\leq$70 ns

Electrical Parts List (No. P70024622, Rev. C)

Ref. Desig.	Description	Part No.
C1	CAPACITOR, FIXED, ELECTROLYTIC, TANTALUM: 1.5 µF ± 20%, 20 Vdc	70 930 230 009
M1, M3, M5, M7	MICROCIRCUIT: F-03, power amplifier integrated circuit	70 950 100 003
M2, M4, M6, M8	MICROCIRCUIT: 949, NAND gate integrated circuit	70 950 105 010
R1-R6 (CC-819A)	RESISTOR, FIXED, COMPOSITION: 100 ohms ± 5%, 1/4W	70 932 007 025
R7 (CC-819A)	RESISTOR, FIXED, COMPOSITION: 12 ohms ±5%, 1/4W	70 932 007 003
R1-R6 (CM-493)	RESISTOR, FIXED, COMPOSITION: 62 ohms ±5%, 1/4W	70 932 007 003

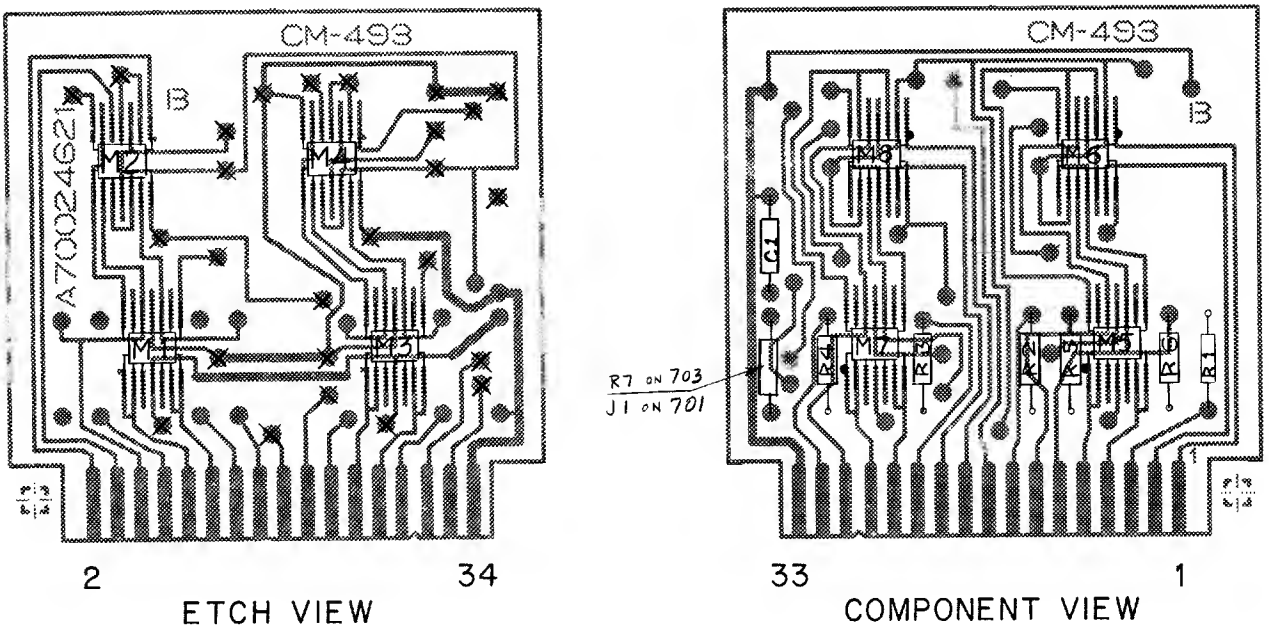


Figure 1. Data Register PAC, Models CM-493/CC-819A
Parts Location (Dwg A70024622, Rev. C)

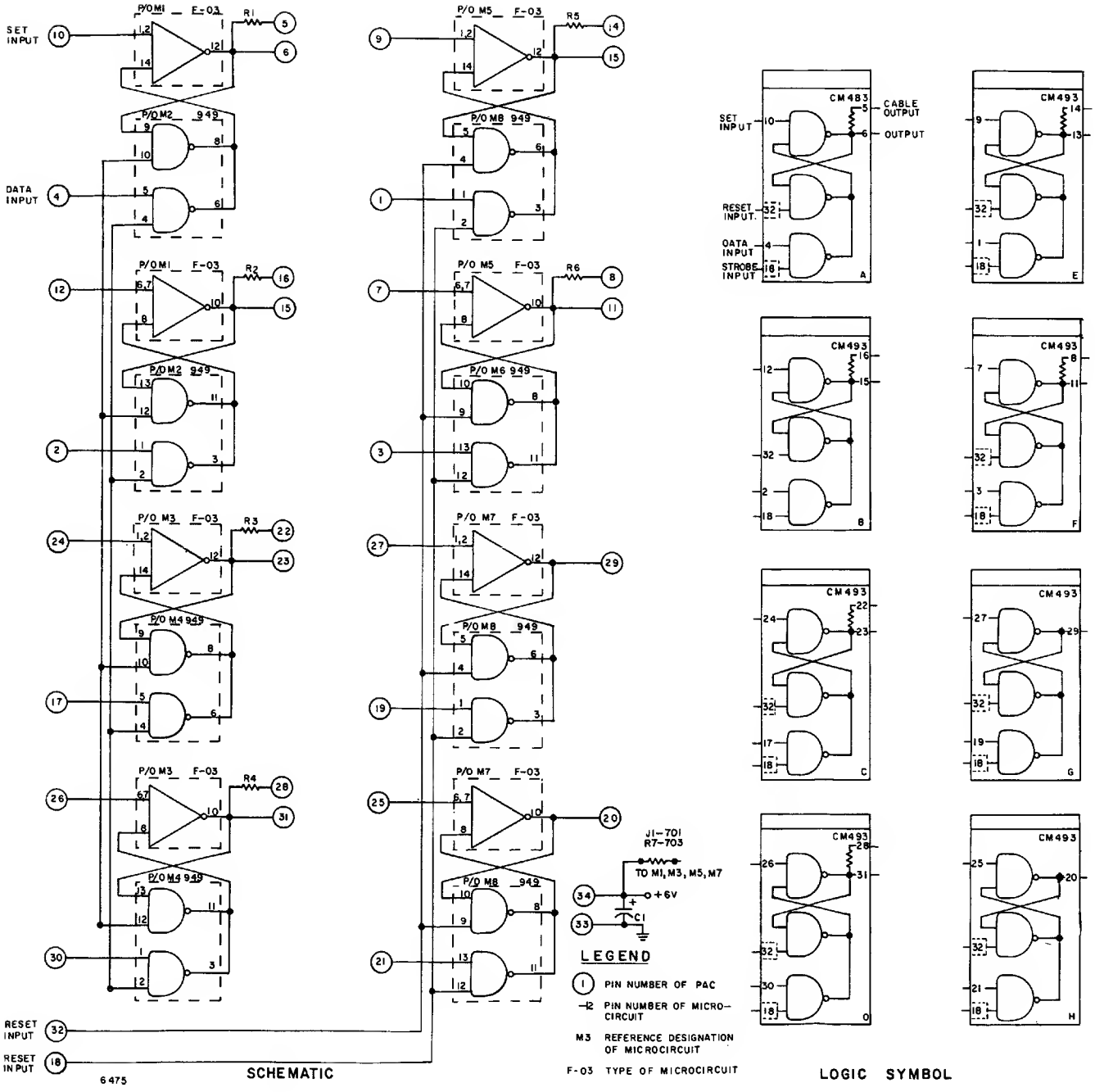


Figure 2. Data Register PAC, Models CM-493/CC-819A, Schematic Diagram and Logic Symbol (Dwg B70024622, Rev. A)

FIELD ENGINEERING MANUAL
USERS' REMARKS FORM

TITLE:

DOC. PART NO. _____

DATED _____

ERRORS NOTED:

Fold

SUGGESTIONS FOR IMPROVEMENT:

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DATE _____

FROM: NAME _____

COMPANY _____ M/S _____

TITLE _____

ADDRESS _____

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